



# **HT32F12345**

## **Datasheet**

**32-Bit Arm® Cortex®-M3 Microcontroller,  
up to 64 KB Flash and 16 KB SRAM with 1 MSPS ADC,  
USART, UART, SPI, I<sup>2</sup>C, I<sup>2</sup>S, MCTM, GPTM, BFTM,  
PDMA, CRC, RTC, WDT, EBI, SDIO and USB2.0 FS**

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# 1 General Description

The HOLTEK HT32F12345 device is a high performance, low power consumption 32-bit microcontroller based around an Arm® Cortex®-M3 processor core. The Cortex®-M3 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and includes advanced debug support.

The device operates at a frequency of up to 96 MHz with a Flash accelerator to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code/data storage and 16 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I<sup>2</sup>C, USART, UART, SPI, I<sup>2</sup>S, PDMA, GPTM, MCTM, EBI, CRC-16/32, SDIO, USB2.0 FS and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition and so on.

**arm** CORTEX

## 2 Features

### Core

- 32-bit Arm® Cortex®-M3 processor core
- Up to 96 MHz operating frequency
- Single-cycle multiplication and hardware division
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many special features such as a Thumb-2 instruction set, hardware divider, low latency interrupt respond time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex®-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets.

### On-chip Memory

- 64 KB on-chip Flash memory for instruction/data and option storage
- 16 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M3 processor is structured using Harvard architecture which uses a separate bus structure to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex®-M3 is 4 GB due to its 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M3 processor to reduce the software complexity of repeated implementation for different device vendors. However, some regions are used by the Arm® Cortex®-M3 system peripherals. Refer to the Arm® Cortex®-M3 Technical Reference Manual for more information. Figure 2 shows the memory map of the HT32F12345 device, including Code, SRAM, peripheral, and other pre-defined regions.

### Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

## Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

## Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32.768 kHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to  $\pm 2\%$  accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M3 are derived from the system clock (CK\_SYS) which can come from the LSI, LSE, HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK\_AHB) can be up to 96 MHz.

## Power Management – PWRCU

- Single  $V_{DD}$  power supply: 2.0 V to 3.6 V
- Integrated 1.5V LDO regulator for CPU core, peripherals and memories power supply
- $V_{BAT}$  battery power supply for RTC and backup registers
- Three power domains:  $V_{DD}$ ,  $V_{CORE}$  and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.



## External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

## Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 12 external analog input channels
- External reference voltage input possibility

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 12 external analog signal channels and 2 internal channels can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

## Analog Comparator – CMP

- Two rail-to-rail comparators
- Each comparator has configurable negative inputs used for flexible voltage selection
- Dedicated I/O pin or internal voltage reference provided by 6-bit scaler
- Programmable hysteresis
- Programming speed and consumption
- Comparator output can be output to I/O or to timers or ADC trigger inputs
- 6-bit scaler can be configurable to dedicated I/O for voltage reference
- Comparator has interrupt generation capability with wakeup MCU from Sleep or Deep Sleep modes through the EXTI controller

The two general purpose comparators (CMP) are implemented within the device. They can be configured either as standalone comparators or combined with the different kinds of peripheral IP. Each comparator is capable of asserting interrupts to the NVIC or wakeup the MCU Sleep or Deep Sleep modes through EXTI wakeup event management unit.

## I/O Ports – GPIO

- Up to 51 GPIOs
- Port A, B, C, D are mapped as 16 external interrupts – EXTI
- Almost I/O pins are configurable output driving current

There are up to 51 General Purpose I/O pins, GPIO, named from PA0 ~ PA15 to PD0 ~ PD2 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

## Motor Control Timer – MCTM

- One 16-bit up, down, up/down auto-reload counters
- 16-bit programmable prescaler allowing division of the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with edge aligned and center-aligned Counting Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Encoder interface controller with two inputs using quadrature decoder
- Supports 3-phase motor control and hall sensor interface
- Brake input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of a single 16-bit up/down counter; four 16-bit CCRs (Capture/Compare Registers), single 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM supports an Encoder interface controller to an incremental encoder with two inputs. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

## General-Purpose Timer – GPTM

- One 16-bit up, down, up/down auto-reload counters
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes

- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General Purpose Timer consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

## Basic Function Timer – BFTM

- One 32-bit compare/match count-up counters - no I/O control features
- One shot mode - counting stops after a match condition
- Repetitive mode - restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

## Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Interrupt or reset event for the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and a WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before a Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

## Real Time Clock – RTC

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC for short, includes an APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V<sub>CORE</sub> power

domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the  $V_{CORE}$  power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

## Inter-integrated Circuit – I<sup>2</sup>C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I<sup>2</sup>C Module is an internal circuit allowing communication with an external I<sup>2</sup>C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I<sup>2</sup>C module provides three data transfer rates: (1) 100 kHz in the Standard mode, (2) 400 kHz in the Fast mode and (3) 1 MHz in the Fast mode plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I<sup>2</sup>C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I<sup>2</sup>C module also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I<sup>2</sup>C bus at the same time.

## Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to ( $f_{PCLK}/2$ ) MHz for master mode and ( $f_{PCLK}/3$ ) MHz for slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, which are the serial data input and output lines, MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

## Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Asynchronous operating baud rate up to ( $f_{PCLK}/16$ ) MHz and synchronous operating rate up to ( $f_{PCLK}/8$ ) MHz
- Full duplex communication

- Fully programmable serial communication characteristics including
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX\_FIFO) and a receiver FIFO (RX\_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate up to ( $f_{CLK}/16$ ) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

## Inter-IC Sound – I<sup>2</sup>S

- Master or slave mode
- Mono and stereo
- I2S-justified, Left-justified, and Right-justified mode
- 8/16/24/32-bit sample size with 32-bit channel extended

- 8 × 32-bits Tx & Rx FIFO with PDMA supported
- 8-bit Fractional Clock Divider with rate control

The I<sup>2</sup>S is a synchronous communication interface that can be used as a master or slave to exchange data with other audio peripherals, such as ADCs or DACs. The I<sup>2</sup>S supports a variety of data formats. In addition to the stereo I2S-justified, Left-justified and Right-justified modes, there are mono PCM modes with 8/16/24/32-bit sample size. When the I<sup>2</sup>S operates in the master mode, then when using the fractional divider, it can provide an accurate sampling frequency output and support the rate control function and fine-tuning of the output frequency to avoid system problems caused by the cumulative frequency error between different devices.

## Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,  
 $X^{16}+X^{15}+X^2+1$
- Supports CCITT CRC16 polynomial: 0x1021,  
 $X^{16}+X^{12}+X^5+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,  
 $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as input and generates a 16-bit or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means data stream contains a data error.

## Peripheral Direct Memory Access – PDMA

- 12 channels with trigger source grouping
- 8/16/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source:

ADC, SPI, EBI, CRC, USART, UART, I<sup>2</sup>C, I<sup>2</sup>S, GPTM, MCTM, SDIO and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt

service routine execution. It improves system performance as the software does not need to join each data movement operation.

## External Bus Interface – EBI

- Programmable interface for various memory types
- Translate the AHB transactions into the appropriate external device protocol
- Memory bank regions and independent chip select control for each memory bank
- Programmable timings to support a wide range of devices
- Includes page read mode
- Automatic translation when the AHB transaction width and external memory interface width is different
- Write buffer to decrease the stalling of the AHB write burst transaction
- Multiplexed and non-multiplexed address and data line configurations
  - Up to 21 address lines
  - Up to 16-bit data bus width

The external bus interface is able to access external parallel interface devices such as SRAM, Flash and LCD modules. The interface is memory mapped into the internal address map of the CPU. The data and address lines are multiplexed in order to reduce the number of pins required to connect to the external devices. The read/write timing of the bus can be adjusted to meet the timing specification of the external devices. Note the interface only supports asynchronous 8-bit or 16-bit bus interface.

## Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12 Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1024-byte EP-SRAM used as the endpoint data buffers

The USB device controller is compliant with the USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffer. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimize the overall system complexity and cost. The USB functional block also contains the resume and suspend feature to meet the requirements of low-power consumption.

## Secure Digital Input Output – SDIO

- Supports two different data bus modes: 1-bit (default) and 4-bit
- Supports two different speed modes: Normal speed (default) and High speed
- SD clock frequency of up to 48 MHz
- SPI mode and MMC stream mode not supported

The SDIO includes a command register, argument register, response registers, data buffer, timeout counter and error detection logic. The SDIO supports single block and multi-block data transfers and is compatible with the PDMA, minimizing processor intervention for large data transfers.

## Debug Support

- Serial Wire Debug Port SW-DP
- 6 instruction comparators and 2 literal comparators for hardware breakpoint or code / literal patches
- 4 comparators for hardware watchpoints
- 1-bit asynchronous trace for serial wire debug mode – TRACESWO

## Package and Operation Temperature

- 48/64-pin LQFP packages
- Operation temperature range: -40 °C to 85 °C



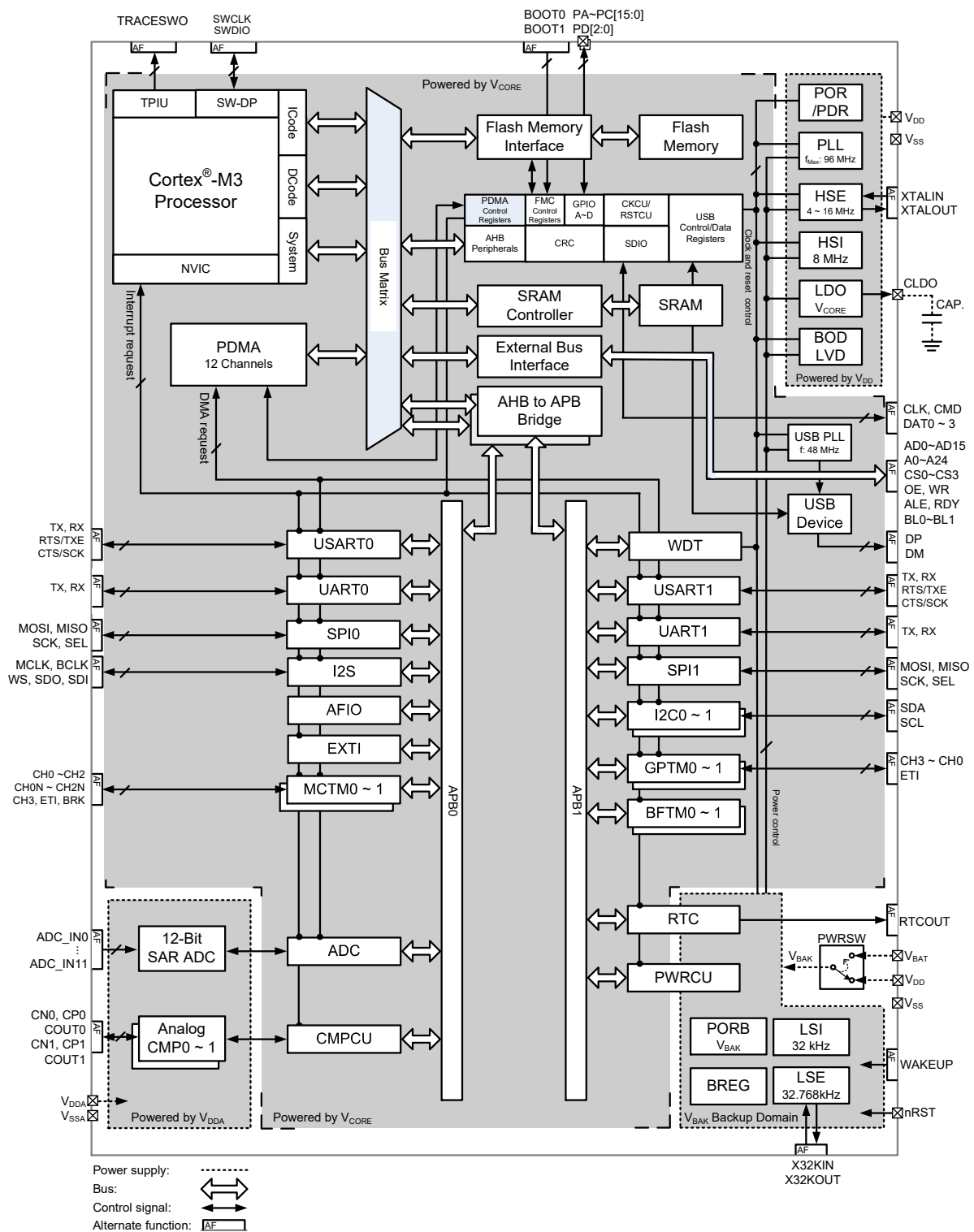
# 3 Overview

## Device Information

**Table 1. Features and Peripheral List**

| Peripherals            |                  | HT32F12345       |
|------------------------|------------------|------------------|
| Main Flash (KB)        |                  | 63               |
| Option Byte Flash (KB) |                  | 1                |
| SRAM (KB)              |                  | 16               |
| Timers                 | MCTM             | 2                |
|                        | GPTM             | 2                |
|                        | BFTM             | 2                |
|                        | RTC              | 1                |
|                        | WDT              | 1                |
| Communication          | USB              | 1                |
|                        | USART            | 2                |
|                        | UART             | 2                |
|                        | SPI              | 2                |
|                        | I <sup>2</sup> C | 2                |
|                        | I <sup>2</sup> S | 1                |
| PDMA                   |                  | 12 channels      |
| SDIO                   |                  | 1                |
| EBI                    |                  | 1                |
| CRC                    |                  | 1                |
| GPIO                   |                  | Up to 51         |
| EXTI                   |                  | 16               |
| 12-bit ADC             |                  | 1                |
| Number of channels     |                  | Max. 12 Channels |
| Comparator             |                  | 2                |
| CPU frequency          |                  | Up to 96 MHz     |
| Operating voltage      |                  | 2.0 V ~ 3.6 V    |
| Operating temperature  |                  | -40 °C ~ 85 °C   |
| Package                |                  | 48/64-pin LQFP   |

## Block Diagram



**Figure 1. Block Diagram**

## Memory Map

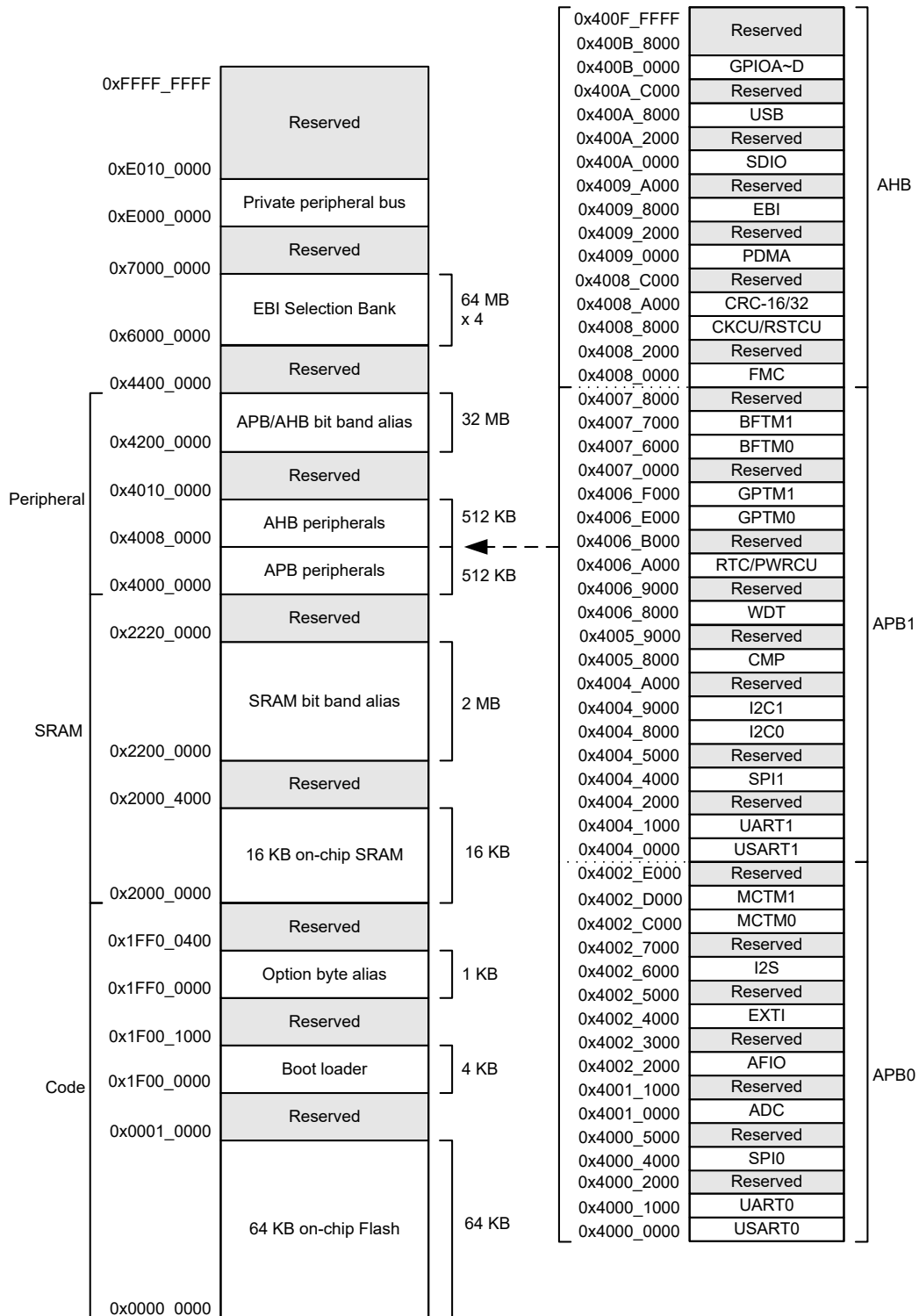


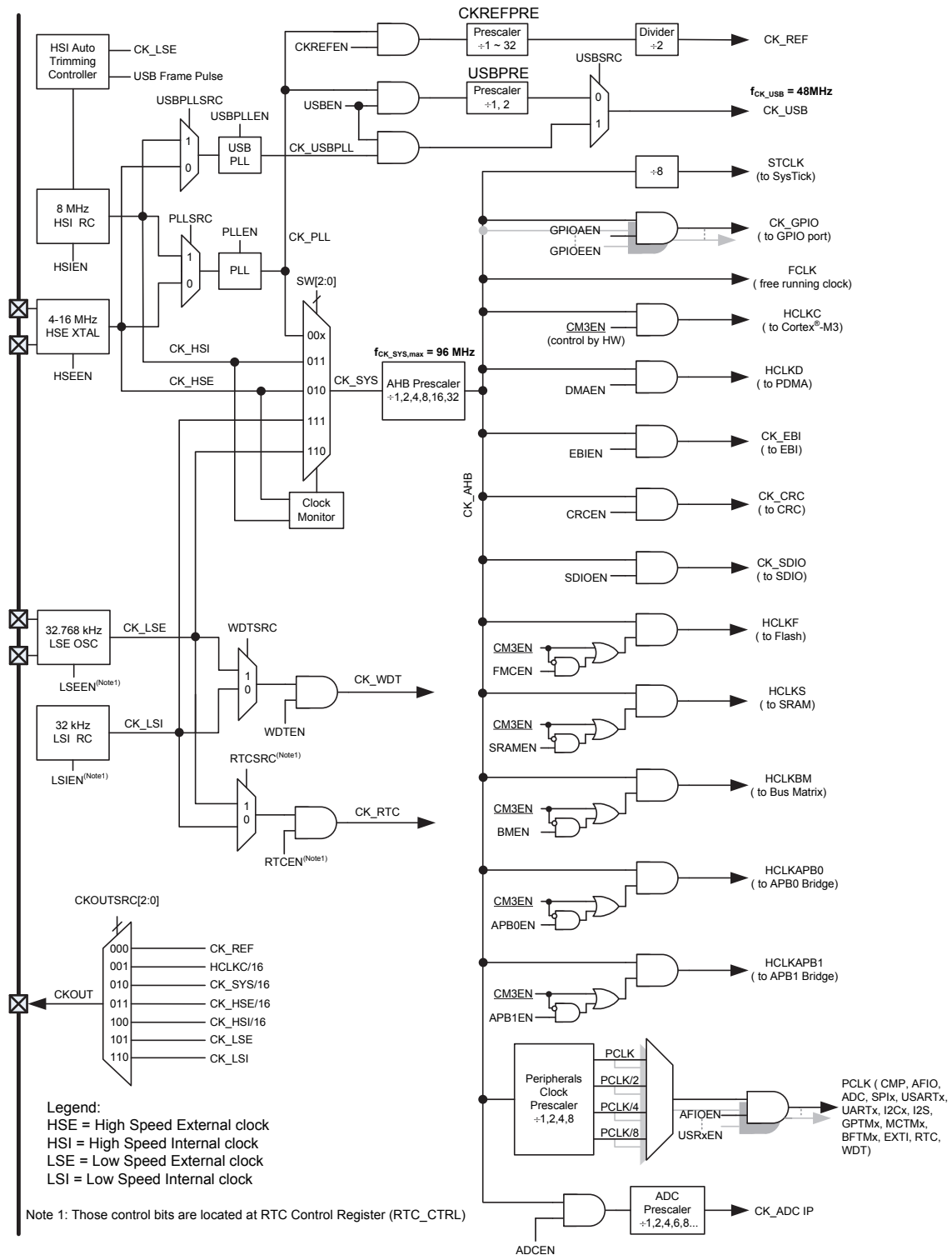
Figure 2. Memory Map

**Table 2. Register Map**

| Start Address | End Address | Peripheral | Bus  |
|---------------|-------------|------------|------|
| 0x4000_0000   | 0x4000_0FFF | USART0     | APB0 |
| 0x4000_1000   | 0x4000_1FFF | UART0      |      |
| 0x4000_2000   | 0x4000_3FFF | Reserved   |      |
| 0x4000_4000   | 0x4000_4FFF | SPI0       |      |
| 0x4000_5000   | 0x4000_FFFF | Reserved   |      |
| 0x4001_0000   | 0x4001_0FFF | ADC        |      |
| 0x4001_1000   | 0x4002_1FFF | Reserved   |      |
| 0x4002_2000   | 0x4002_2FFF | AFIO       |      |
| 0x4002_3000   | 0x4002_3FFF | Reserved   |      |
| 0x4002_4000   | 0x4002_4FFF | EXTI       |      |
| 0x4002_5000   | 0x4002_5FFF | Reserved   |      |
| 0x4002_6000   | 0x4002_6FFF | I2S        |      |
| 0x4002_7000   | 0x4002_BFFF | Reserved   |      |
| 0x4002_C000   | 0x4002_CFFF | MCTM0      |      |
| 0x4002_D000   | 0x4002_DFFF | MCTM1      |      |
| 0x4002_E000   | 0x4003_FFFF | Reserved   |      |
| 0x4004_0000   | 0x4004_0FFF | USART1     | APB1 |
| 0x4004_1000   | 0x4004_1FFF | UART1      |      |
| 0x4004_2000   | 0x4004_3FFF | Reserved   |      |
| 0x4004_4000   | 0x4004_4FFF | SPI1       |      |
| 0x4004_5000   | 0x4004_7FFF | Reserved   |      |
| 0x4004_8000   | 0x4004_8FFF | I2C0       |      |
| 0x4004_9000   | 0x4004_9FFF | I2C1       |      |
| 0x4004_A000   | 0x4005_7FFF | Reserved   |      |
| 0x4005_8000   | 0x4005_8FFF | CMP        |      |
| 0x4005_9000   | 0x4006_7FFF | Reserved   |      |
| 0x4006_8000   | 0x4006_8FFF | WDT        |      |
| 0x4006_9000   | 0x4006_9FFF | Reserved   |      |
| 0x4006_A000   | 0x4006_AFFF | RTC/PWRCU  |      |
| 0x4006_B000   | 0x4006_DFFF | Reserved   |      |
| 0x4006_E000   | 0x4006_EFFF | GPTM0      |      |
| 0x4006_F000   | 0x4006_FFFF | GPTM1      |      |
| 0x4007_0000   | 0x4007_5FFF | Reserved   |      |
| 0x4007_6000   | 0x4007_6FFF | BFTM0      |      |
| 0x4007_7000   | 0x4007_7FFF | BFTM1      |      |
| 0x4007_8000   | 0x4007_FFFF | Reserved   |      |

| Start Address | End Address | Peripheral             | Bus |
|---------------|-------------|------------------------|-----|
| 0x4008_0000   | 0x4008_1FFF | FMC                    | AHB |
| 0x4008_2000   | 0x4008_7FFF | Reserved               |     |
| 0x4008_8000   | 0x4008_9FFF | CKCU/RSTCU             |     |
| 0x4008_A000   | 0x4008_BFFF | CRC-16/32              |     |
| 0x4008_C000   | 0x4008_FFFF | Reserved               |     |
| 0x4009_0000   | 0x4009_1FFF | PDMA Control Registers |     |
| 0x4009_2000   | 0x4009_7FFF | Reserved               |     |
| 0x4009_8000   | 0x4009_9FFF | EBI Control Registers  |     |
| 0x4009_A000   | 0x4009_FFFF | Reserved               |     |
| 0x400A_0000   | 0x400A_1FFF | SDIO                   |     |
| 0x400A_2000   | 0x400A_7FFF | Reserved               |     |
| 0x400A_8000   | 0x400A_9FFF | USB Control Registers  |     |
| 0x400A_A000   | 0x400A_BFFF | USB SRAM               |     |
| 0x400A_C000   | 0x400A_FFFF | Reserved               |     |
| 0x400B_0000   | 0x400B_1FFF | GPIOA                  |     |
| 0x400B_2000   | 0x400B_3FFF | GPIOB                  |     |
| 0x400B_4000   | 0x400B_5FFF | GPIOC                  |     |
| 0x400B_6000   | 0x400B_7FFF | GPIOD                  |     |
| 0x400B_8000   | 0x400F_FFFF | Reserved               |     |

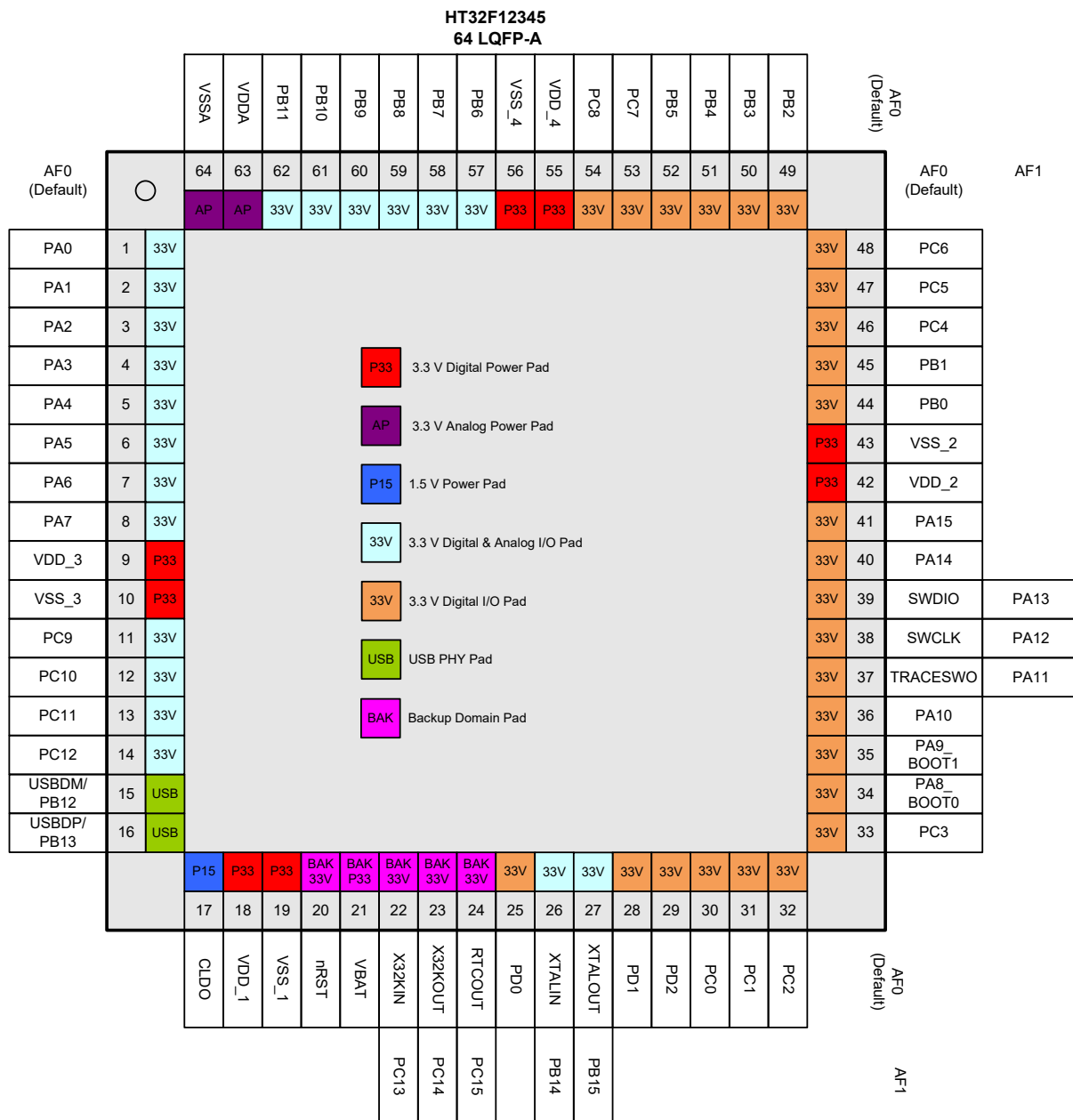
## Clock Structure



**Figure 3. Clock Structure**

## 4 Pin Assignment







**Table 3. Pin Assignment**

| Package |         | Alternate Function Mapping |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
|---------|---------|----------------------------|------|----------|-----|------------|-----------|-------------|------------------|-----|----------|----------|---------|------|------|------|--------------|
|         |         | AF0                        | AF1  | AF2      | AF3 | AF4        | AF5       | AF6         | AF7              | AF8 | AF9      | AF10     | AF11    | AF12 | AF13 | AF14 | AF15         |
| 64 LQFP | 48 LQFP | System Default             | GPIO | ADC      | CMP | MCTM /GPTM | SPI       | USART /UART | I <sup>2</sup> C | N/A | EBI      | I2S      | SDIO    | N/A  | N/A  | N/A  | System Other |
| 1       | 1       | PA0                        |      | ADC_IN0  |     | GT1_CH0    | SPI1_SCK  | USR0_RTS    | I2C1_SCL         |     |          | I2S_WS   |         |      |      |      |              |
| 2       | 2       | PA1                        |      | ADC_IN1  |     | GT1_CH1    | SPI1_MOSI | USR0_CTS    | I2C1_SDA         |     |          | I2S_BCLK | SD_DAT1 |      |      |      |              |
| 3       | 3       | PA2                        |      | ADC_IN2  |     | GT1_CH2    | SPI1_MISO | USR0_TX     |                  |     |          | I2S_SDO  | SD_DAT2 |      |      |      |              |
| 4       | 4       | PA3                        |      | ADC_IN3  |     | GT1_CH3    | SPI1_SEL  | USR0_RX     |                  |     |          | I2S_SDI  | SD_DAT3 |      |      |      |              |
| 5       | 5       | PA4                        |      | ADC_IN4  |     | GT0_CH0    | SPI0_SCK  | USR1_TX     | I2C0_SCL         |     |          |          | SD_CMD  |      |      |      |              |
| 6       | 6       | PA5                        |      | ADC_IN5  |     | GT0_CH1    | SPI0_MOSI | USR1_RX     | I2C0_SDA         |     |          |          | SD_CLK  |      |      |      |              |
| 7       | 7       | PA6                        |      | ADC_IN6  |     | GT0_CH2    | SPI0_MISO | USR1_RTS    |                  |     |          |          | SD_DAT0 |      |      |      |              |
| 8       | 8       | PA7                        |      | ADC_IN7  |     | GT0_CH3    | SPI0_SEL  | USR1_CTS    |                  |     |          | I2S_MCLK |         |      |      |      |              |
| 9       | 9       | VDD_3                      |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 10      | 10      | VSS_3                      |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 11      |         | PC9                        |      | ADC_IN8  |     | GT0_CH0    | SPI1_SEL  | UR0_TX      | I2C1_SCL         |     | EBI_A19  |          | SD_DAT0 |      |      |      |              |
| 12      |         | PC10                       |      | ADC_IN9  |     | GT0_CH1    | SPI1_SCK  | UR0_RX      | I2C1_SDA         |     | EBI_A20  |          | SD_DAT1 |      |      |      |              |
| 13      |         | PC11                       |      | ADC_IN10 |     | GT0_CH2    | SPI1_MOSI |             |                  |     | EBI_A0   |          | SD_DAT2 |      |      |      |              |
| 14      |         | PC12                       |      | ADC_IN11 |     | GT0_CH3    | SPI1_MISO |             |                  |     | EBI_A1   |          | SD_DAT3 |      |      |      |              |
| 15      | 11      | PB12                       |      |          |     | MT1_CH2    |           | USR0_TX     | I2C0_SCL         |     |          |          |         |      |      |      |              |
| 15      | 11      | USBDM                      |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 16      | 12      | USBDP                      |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 16      | 12      | PB13                       |      |          |     | MT1_CH2N   |           | USR0_RX     | I2C0_SDA         |     |          |          |         |      |      |      |              |
| 17      | 13      | CLDO                       |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 18      | 14      | VDD_1                      |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 19      | 15      | VSS_1                      |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 20      | 16      | nRST                       |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 21      | 17      | VBAT                       |      |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 22      | 18      | X32KIN                     | PC13 |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 23      | 19      | X32KOUT                    | PC14 |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 24      | 20      | RTCOUT                     | PC15 |          |     |            |           |             |                  |     |          |          |         |      |      |      | WAKEUP       |
| 25      |         | PD0                        |      |          |     | MT1_ETI    |           |             | I2C0_SDA         |     | EBI_A18  | I2S_SDI  | SD_CMD  |      |      |      |              |
| 26      | 21      | XTALIN                     | PB14 |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 27      | 22      | XTALOUT                    | PB15 |          |     |            |           |             |                  |     |          |          |         |      |      |      |              |
| 28      | 23      | PD1                        |      |          |     | MT1_CH0    | SPI0_SEL  |             | I2C1_SCL         |     | EBI_A16  | I2S_MCLK | SD_CLK  |      |      |      |              |
| 29      | 24      | PD2                        |      |          |     | MT1_CH0N   | SPI0_SCK  |             | I2C1_SDA         |     | EBI_A17  |          | SD_CMD  |      |      |      |              |
| 30      |         | PC0                        |      |          |     | GT1_CH0    | SPI1_SEL  |             |                  |     | EBI_AD13 | I2S_WS   | SD_DAT1 |      |      |      |              |
| 31      |         | PC1                        |      |          |     | GT1_CH1    | SPI1_SCK  |             |                  |     | EBI_AD14 | I2S_BCLK | SD_DAT2 |      |      |      |              |
| 32      |         | PC2                        |      |          |     | GT1_CH2    | SPI1_MOSI | UR1_TX      | I2C0_SCL         |     | EBI_AD15 | I2S_SDO  | SD_DAT3 |      |      |      |              |
| 33      |         | PC3                        |      |          |     | GT1_CH3    | SPI1_MISO | UR1_RX      | I2C0_SDA         |     | EBI_CS3  | I2S_SDI  | SD_DAT0 |      |      |      |              |
| 34      | 25      | PA8_BOOT0                  |      |          |     | GT0_ETI    |           | USR0_TX     |                  |     |          | I2S_MCLK |         |      |      |      | CKOUT        |

| Package |         | Alternate Function Mapping |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
|---------|---------|----------------------------|------|-----|-------|------------|-----------|-------------|------------------|-----|----------|----------|---------|------|------|------|--------------|
|         |         | AF0                        | AF1  | AF2 | AF3   | AF4        | AF5       | AF6         | AF7              | AF8 | AF9      | AF10     | AF11    | AF12 | AF13 | AF14 | AF15         |
| 64 LQFP | 48 LQFP | System Default             | GPIO | ADC | CMP   | MCTM /GPTM | SPI       | USART /UART | I <sup>2</sup> C | N/A | EBI      | I2S      | SDIO    | N/A  | N/A  | N/A  | System Other |
| 35      | 26      | PA9_BOOT1                  |      |     |       |            | SPI0_MOSI |             |                  |     | EBI_A1   | I2S_WS   |         |      |      |      |              |
| 36      | 27      | PA10                       |      |     |       | MT1_CH1    |           | USR0_RX     |                  |     |          |          | SD_DAT0 |      |      |      |              |
| 37      | 28      | TRACESWO                   | PA11 |     |       | MT1_CH1N   | SPI0_MISO |             |                  |     | EBI_A0   | I2S_MCLK |         |      |      |      |              |
| 38      | 29      | SWCLK                      | PA12 |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 39      | 30      | SWDIO                      | PA13 |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 40      | 31      | PA14                       |      |     |       | MT0_CH0    | SPI1_SEL  | USR1_TX     |                  |     | EBI_AD0  |          |         |      |      |      |              |
| 41      | 32      | PA15                       |      |     |       | MT0_CH0N   | SPI1_SCK  | USR1_RX     |                  |     | EBI_AD1  |          |         |      |      |      |              |
| 42      |         | VDD_2                      |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 43      |         | VSS_2                      |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 44      | 33      | PB0                        |      |     |       | MT0_CH1    | SPI1_MOSI | USR0_TX     | I2C0_SCL         |     | EBI_AD2  |          |         |      |      |      |              |
| 45      | 34      | PB1                        |      |     |       | MT0_CH1N   | SPI1_MISO | USR0_RX     | I2C0_SDA         |     | EBI_AD3  |          |         |      |      |      |              |
| 46      |         | PC4                        |      |     |       | MT1_CH2    |           | USR1_RTS    |                  |     | EBI_AD10 |          | SD_CLK  |      |      |      |              |
| 47      |         | PC5                        |      |     |       | MT1_CH2N   |           | USR1_CTS    |                  |     | EBI_AD11 |          | SD_CMD  |      |      |      |              |
| 48      |         | PC6                        |      |     |       | MT1_CH3    |           |             |                  |     | EBI_AD12 |          | SD_DAT0 |      |      |      |              |
|         | 35      | VDD_2                      |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
|         | 36      | VSS_2                      |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 49      | 37      | PB2                        |      |     |       | MT0_CH2    | SPI0_SEL  | UR0_TX      |                  |     | EBI_AD4  |          |         |      |      |      |              |
| 50      | 38      | PB3                        |      |     |       | MT0_CH2N   | SPI0_SCK  | UR0_RX      |                  |     | EBI_AD5  |          |         |      |      |      |              |
| 51      | 39      | PB4                        |      |     |       | MT0_BRK    | SPI0_MOSI | UR1_TX      |                  |     | EBI_AD6  |          |         |      |      |      |              |
| 52      | 40      | PB5                        |      |     |       | MT1_BRK    | SPI0_MISO | UR1_RX      |                  |     | EBI_AD7  |          |         |      |      |      |              |
| 53      |         | PC7                        |      |     |       | MT0_CH3    |           |             | I2C0_SCL         |     | EBI_AD8  |          | SD_CMD  |      |      |      |              |
| 54      |         | PC8                        |      |     |       | MT0_ETI    |           |             | I2C0_SDA         |     | EBI_AD9  |          | SD_CLK  |      |      |      |              |
| 55      |         | VDD_4                      |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 56      |         | VSS_4                      |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 57      | 41      | PB6                        |      |     | CN0   | MT1_CH0    | SPI1_SEL  | UR1_TX      |                  |     | EBI_OE   | I2S_MCLK |         |      |      |      |              |
| 58      | 42      | PB7                        |      |     | CP0   | MT1_CH0N   | SPI1_SCK  |             |                  |     | EBI_CS0  |          |         |      |      |      |              |
| 59      | 43      | PB8                        |      |     | COUT0 | GT1_ETI    | SPI1_MOSI | UR1_RX      |                  |     | EBI_WE   |          |         |      |      |      |              |
| 60      | 44      | PB9                        |      |     | CN1   | MT1_CH2    | SPI1_MISO | UR0_TX      |                  |     | EBI_ALE  | I2S_BCLK | SD_DAT1 |      |      |      |              |
| 61      | 45      | PB10                       |      |     | CP1   | MT1_CH2N   |           |             | I2C1_SCL         |     | EBI_CS1  | I2S_SDO  | SD_DAT2 |      |      |      |              |
| 62      | 46      | PB11                       |      |     | COUT1 | MT1_CH3    |           | UR0_RX      | I2C1_SDA         |     | EBI_CS2  | I2S_SDI  | SD_DAT3 |      |      |      |              |
| 63      | 47      | VDDA                       |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |
| 64      | 48      | VSSA                       |      |     |       |            |           |             |                  |     |          |          |         |      |      |      |              |

**Table 4. Pin Description**

| Pin Number |         | Pin Name            | Type <sup>(1)</sup>   | I/O Structure <sup>(2)</sup> | Output Driving | Description   |
|------------|---------|---------------------|-----------------------|------------------------------|----------------|---|
| 64 LQFP    | 48 LQFP |                     |                       |                              |                | Default Function (AF0)  |
| 1          | 1       | PA0                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA0   |
| 2          | 2       | PA1                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA1   |
| 3          | 3       | PA2                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA2, this pin provides a UART_TX function in the Boot loader mode.  |
| 4          | 4       | PA3                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA3, this pin provides a UART_RX function in the Boot loader mode.  |
| 5          | 5       | PA4                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA4   |
| 6          | 6       | PA5                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA5   |
| 7          | 7       | PA6                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA6   |
| 8          | 8       | PA7                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PA7   |
| 9          | 9       | VDD_3               | P                     | —                            | —              | Voltage for digital I/O   |
| 10         | 10      | VSS_3               | P                     | —                            | —              | Ground reference for digital I/O  |
| 11         |         | PC9                 | AI/O                  | 33V                          | 4/8/12/16 mA   | PC9   |
| 12         |         | PC10                | AI/O                  | 33V                          | 4/8/12/16 mA   | PC10  |
| 13         |         | PC11                | AI/O                  | 33V                          | 4/8/12/16 mA   | PC11  |
| 14         |         | PC12                | AI/O                  | 33V                          | 4/8/12/16 mA   | PC12  |
| 15         | 11      | PB12                | I/O                   | 33V                          | 4/8/12/16 mA   | PB12  |
| 15         | 11      | USBDM               | AI/O                  | —                            | —              | USB Differential data bus conforming to the Universal Serial Bus standard   |
| 16         | 12      | USBDP               | AI/O                  | —                            | —              | USB Differential data bus conforming to the Universal Serial Bus standard   |
| 16         | 12      | PB13                | I/O                   | 33V                          | 4/8/12/16 mA   | PB13  |
| 17         | 13      | CLDO                | P                     | —                            | —              | Core power LDO V <sub>CORE</sub> output.<br>It must be connected an external capacitor as close as possible between this pin and VSS_1. |
| 18         | 14      | VDD_1               | P                     | —                            | —              | Voltage for digital I/O   |
| 19         | 15      | VSS_1               | P                     | —                            | —              | Ground reference for digital I/O  |
| 20         | 16      | nRST                | I(BK <sup>(1)</sup> ) | 33V_PU                       | —              | External reset pin and external wakeup pin in the Power-Down mode   |
| 21         | 17      | VBAT                | P                     | —                            | —              | Battery power input for the backup domain   |
| 22         | 18      | PC13 <sup>(4)</sup> | AI/O(BK)              | 33V                          | < 2 mA         | X32KIN  |
| 23         | 19      | PC14 <sup>(4)</sup> | AI/O(BK)              | 33V                          | < 2 mA         | X32KOUT   |
| 24         | 20      | PC15 <sup>(4)</sup> | I/O(BK)               | 33V                          | < 2 mA         | RTCOUT  |
| 25         |         | PD0                 | I/O                   | 33V                          | 4/8/12/16 mA   | PD0   |
| 26         | 21      | PB14                | AI/O                  | 33V                          | 4/8/12/16 mA   | XTALIN  |
| 27         | 22      | PB15                | AI/O                  | 33V                          | 4/8/12/16 mA   | XTALOUT   |
| 28         | 23      | PD1                 | I/O                   | 33V                          | 4/8/12/16 mA   | PD1   |
| 29         | 24      | PD2                 | I/O                   | 33V                          | 4/8/12/16 mA   | PD2   |
| 30         |         | PC0                 | I/O                   | 33V                          | 4/8/12/16 mA   | PC0   |
| 31         |         | PC1                 | I/O                   | 33V                          | 4/8/12/16 mA   | PC1   |
| 32         |         | PC2                 | I/O                   | 33V                          | 4/8/12/16 mA   | PC2   |
| 33         |         | PC3                 | I/O                   | 33V                          | 4/8/12/16 mA   | PC3   |
| 34         | 25      | PA8                 | I/O                   | 33V_PU                       | 4/8/12/16 mA   | PA8_BOOT0   |
| 35         | 26      | PA9                 | I/O                   | 33V_PU                       | 4/8/12/16 mA   | PA9_BOOT1   |
| 36         | 27      | PA10                | I/O                   | 33V                          | 4/8/12/16 mA   | PA10  |
| 37         | 28      | PA11                | I/O                   | 33V                          | 4/8/12/16 mA   | TRACESWO  |
| 38         | 29      | PA12                | I/O                   | 33V_PU                       | 4/8/12/16 mA   | SWCLK   |

| Pin Number |         | Pin Name | Type <sup>(1)</sup> | I/O Structure <sup>(2)</sup> | Output Driving | Description                                 |
|------------|---------|----------|---------------------|------------------------------|----------------|---|
| 64 LQFP    | 48 LQFP |          |                     |                              |                | Default Function (AF0)                      |
| 39         | 30      | PA13     | I/O                 | 33V_PU                       | 4/8/12/16 mA   | SWDIO                                       |
| 40         | 31      | PA14     | I/O                 | 33V_PU                       | 4/8/12/16 mA   | PA14  |
| 41         | 32      | PA15     | I/O                 | 33V_PU                       | 4/8/12/16 mA   | PA15  |
| 42         |         | VDD_2    | P                   | —                            | —              | Voltage for digital I/O                     |
| 43         |         | VSS_2    | P                   | —                            | —              | Ground reference for digital I/O            |
| 44         | 33      | PB0      | I/O                 | 33V                          | 4/8/12/16 mA   | PB0   |
| 45         | 34      | PB1      | I/O                 | 33V                          | 4/8/12/16 mA   | PB1   |
| 46         |         | PC4      | I/O                 | 33V                          | 4/8/12/16 mA   | PC4   |
| 47         |         | PC5      | I/O                 | 33V                          | 4/8/12/16 mA   | PC5   |
| 48         |         | PC6      | I/O                 | 33V                          | 4/8/12/16 mA   | PC6   |
|            | 35      | VDD_2    | P                   | —                            | —              | Voltage for digital I/O                     |
|            | 36      | VSS_2    | P                   | —                            | —              | Ground reference for digital I/O            |
| 49         | 37      | PB2      | I/O                 | 33V                          | 4/8/12/16 mA   | PB2   |
| 50         | 38      | PB3      | I/O                 | 33V                          | 4/8/12/16 mA   | PB3   |
| 51         | 39      | PB4      | I/O                 | 33V                          | 4/8/12/16 mA   | PB4   |
| 52         | 40      | PB5      | I/O                 | 33V                          | 4/8/12/16 mA   | PB5   |
| 53         |         | PC7      | I/O                 | 33V                          | 4/8/12/16 mA   | PC7   |
| 54         |         | PC8      | I/O                 | 33V                          | 4/8/12/16 mA   | PC8   |
| 55         |         | VDD_4    | P                   | —                            | —              | Voltage for digital I/O                     |
| 56         |         | VSS_4    | P                   | —                            | —              | Ground reference for digital I/O            |
| 57         | 41      | PB6      | AI/O                | 33V                          | 4/8/12/16 mA   | PB6   |
| 58         | 42      | PB7      | AI/O                | 33V                          | 4/8/12/16 mA   | PB7   |
| 59         | 43      | PB8      | AI/O                | 33V                          | 4/8/12/16 mA   | PB8   |
| 60         | 44      | PB9      | AI/O                | 33V                          | 4/8/12/16 mA   | PB9   |
| 61         | 45      | PB10     | AI/O                | 33V                          | 4/8/12/16 mA   | PB10  |
| 62         | 46      | PB11     | AI/O                | 33V                          | 4/8/12/16 mA   | PB11  |
| 63         | 47      | VDDA     | P                   | —                            | —              | Analog voltage for ADC and Comparator       |
| 64         | 48      | VSSA     | P                   | —                            | —              | Ground reference for the ADC and Comparator |

Note: 1. I = Input, O = Output, A = Analog port, P = Power supply, PU = Pull-up, BK = Backup domain.

2. 33V = 3.3 V tolerant.

3. The GPIOs are in an AF0 state after a V<sub>CORE</sub> power on reset (POR) except for the RTCOUT pin in the Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or by the Backup Domain software reset (BAK\_RST bit in BAK\_CR register).

4. The backup domain of the I/O pins have a source current capability limitation of < 2 mA @ V<sub>DD</sub> = 3.3 V and sink current typical is 4/8 mA configurable @ V<sub>DD</sub> = 3.3 V.

5. In the Boot loader mode, the UART and USB interfaces are available for communication.

# 5 Electrical Characteristics

## Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**Table 5. Absolute Maximum Ratings**

| Symbol           | Parameter   | Min.                   | Max.                   | Unit. |
|------------------|---|------------------------|------------------------|-------|
| V <sub>DD</sub>  | External main supply voltage                      | V <sub>SS</sub> - 0.3  | V <sub>SS</sub> + 3.6  | V     |
| V <sub>DDA</sub> | External analog supply voltage                    | V <sub>SSA</sub> - 0.3 | V <sub>SSA</sub> + 3.6 | V     |
| V <sub>BAT</sub> | External battery supply voltage                   | V <sub>SS</sub> - 0.3  | V <sub>SS</sub> + 3.6  | V     |
| V <sub>IN</sub>  | Input voltage on other I/O                        | V <sub>SS</sub> - 0.3  | V <sub>DD</sub> + 0.3  | V     |
| T <sub>A</sub>   | Ambient operating temperature range               | -40                    | 85                     | °C    |
| T <sub>STG</sub> | Storage temperature range                         | -60                    | 150                    | °C    |
| T <sub>J</sub>   | Maximum junction temperature                      | —                      | 125                    | °C    |
| P <sub>D</sub>   | Total power dissipation                           | —                      | 500                    | mW    |
| V <sub>ESD</sub> | Electrostatic discharge voltage - human body mode | -4000                  | 4000                   | V     |

## Recommended DC Operating Conditions

**Table 6. Recommended DC Operating Conditions**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol           | Parameter                        | Conditions | Min. | Typ. | Max. | Unit |
|------------------|----------------------------------|------------|------|------|------|------|
| V <sub>DD</sub>  | I/O operating voltage            | —          | 2.0  | 3.3  | 3.6  | V    |
| V <sub>DDA</sub> | Analog operating voltage         | —          | 2.5  | 3.3  | 3.6  | V    |
| V <sub>BAT</sub> | Battery supply operating voltage | —          | 2.0  | 3.3  | 3.6  | V    |

## On-Chip LDO Voltage Regulator Characteristics

**Table 7. LDO Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol           | Parameter  | Conditions  | Min.  | Typ. | Max. | Unit |
|------------------|--|---|-------|------|------|------|
| V <sub>LDO</sub> | Internal regulator output voltage                              | V <sub>DD</sub> ≥ 2.0 V Regulator input @<br>I <sub>LDO</sub> = 35 mA and voltage variant = ±5 %,<br>After trimming | 1.425 | 1.5  | 1.57 | V    |
| I <sub>LDO</sub> | Output current   | V <sub>DD</sub> = 2.0 V Regulator input @<br>V <sub>LDO</sub> = 1.5 V   | —     | 50   | 75   | mA   |
| C <sub>LDO</sub> | External filter capacitor value for internal core power supply | The Tantalum capacitor value is dependent on the core power current consumption                                     | 2.2   | 4.7  | —    | μF   |
|                  |  | The MLCC capacitor value is dependent on the core power current consumption   | 10    | —    | —    |      |

## Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the  $f_{HCLK}$  frequency.
- When the peripherals are enabled,  $f_{PCLK} = f_{HCLK}$ .

**Table 8. Power Consumption Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol   | Parameter                         | $f_{HCLK}$ | Conditions  | Min. | Typ. | Max. | Unit          |
|----------|-----------------------------------|------------|---|------|------|------|---------------|
| $I_{DD}$ | Supply current (Run mode)         | 96 MHz     | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>HSI = 8 MHz<br>PLL = 96 MHz<br>All peripherals enabled   | —    | 42   | —    | mA            |
|          |                                   |            | All peripherals disabled  | —    | 22   | —    |               |
|          |                                   | 72 MHz     | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>HSI = 8 MHz<br>PLL = 72 MHz<br>All peripherals enabled   | —    | 35   | —    |               |
|          |                                   |            | All peripherals disabled  | —    | 20   | —    |               |
|          |                                   | 48 MHz     | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>HSI = 8 MHz<br>PLL = 96 MHz<br>All peripherals enabled   | —    | 28   | —    |               |
|          |                                   |            | All peripherals disabled  | —    | 17   | —    |               |
|          |                                   | 24 MHz     | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>HSI = 8 MHz<br>PLL = 96 MHz<br>All peripherals enabled   | —    | 17   | —    |               |
|          |                                   |            | All peripherals disabled  | —    | 10   | —    |               |
|          |                                   | 8 MHz      | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>HSI = 8 MHz<br>PLL = off<br>All peripherals enabled  | —    | 8.0  | —    |               |
|          |                                   |            | All peripherals disabled  | —    | 5.0  | —    |               |
|          | Supply current (Sleep mode)       | 96 MHz     | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>HSI = 8 MHz<br>PLL = off<br>All peripherals enabled  | —    | 3.0  | —    | $\mu\text{A}$ |
|          |                                   |            | All peripherals disabled  | —    | 2.7  | —    |               |
| $I_{DD}$ | Supply current (Run mode)         | 32 kHz     | $V_{DD} = V_{BAT} = 3.3\text{ V}$<br>LSI = 32 kHz<br>LDO low current mode<br>All peripherals enabled  | —    | 75   | —    | $\mu\text{A}$ |
|          |                                   |            | All peripherals disabled  | —    | 65   | —    |               |
|          | Supply current (Deep-Sleep1 mode) | —          | $V_{DD} = V_{BAT} = 3.3\text{ V}$ , All clock off (HSI/PLL/ $f_{HCLK}$ ), LDO in low power mode, LSE off, LSI on, RTC on<br>All peripherals enabled | —    | 27.5 | —    | mA            |
|          |                                   |            | All peripherals disabled  | —    | 3.5  | —    |               |
|          | Supply current (Deep-Sleep2 mode) | —          | $V_{DD} = V_{BAT} = 3.3\text{ V}$ , All clock off (HSI/PLL/ $f_{HCLK}$ ), LDO off (DMOS on), LSE off, LSI on, RTC on                                | —    | 30   | —    | $\mu\text{A}$ |
|          | Supply current (Power-Down mode)  | —          | $V_{DD} = V_{BAT} = 3.3\text{ V}$ , LDO off, LSE on, LSI on, RTC on   | —    | 5.0  | —    | $\mu\text{A}$ |
|          | Supply current (Power-Down mode)  | —          | $V_{DD} = V_{BAT} = 3.3\text{ V}$ , LDO off, LSE on, LSI on, RTC on   | —    | 3.1  | —    | $\mu\text{A}$ |
|          |                                   |            | $V_{DD} = V_{BAT} = 3.3\text{ V}$ , LDO off, LSE off, LSI on, RTC off   | —    | 1.6  | —    | $\mu\text{A}$ |

| Symbol           | Parameter                                   | f <sub>HCLK</sub> | Conditions  | Min. | Typ. | Max. | Unit |
|------------------|---|-------------------|---|------|------|------|------|
| I <sub>BAT</sub> | Battery supply current<br>(Power-Down mode) | —                 | V <sub>DD</sub> not present, V <sub>BAT</sub> = 3.3 V, LDO off, LSE on,<br>LSI on, RTC on   | —    | 2.7  | —    | μA   |
|                  |   |                   | V <sub>DD</sub> not present, V <sub>BAT</sub> = 3.3 V, LDO off, LSE off,<br>LSI on, RTC off | —    | 1.3  | —    | μA   |

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.  
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.  
3. RTC means real time clock.  
4. Code = while (1) { 208 NOP } executed in Flash.

## Reset and Supply Monitor Characteristics

**Table 9. V<sub>DD</sub> Power Reset Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol               | Parameter   | Conditions                      | Min. | Typ. | Max. | Unit |
|----------------------|---|---------------------------------|------|------|------|------|
| V <sub>POR</sub>     | Power on reset threshold<br>(Rising Voltage on V <sub>DD</sub> )    | T <sub>A</sub> = -40 °C ~ 85 °C | 1.66 | 1.79 | 1.90 | V    |
| V <sub>PDR</sub>     | Power down reset threshold<br>(Falling Voltage on V <sub>DD</sub> ) |                                 | 1.49 | 1.64 | 1.78 | V    |
| V <sub>PORHYST</sub> | POR hysteresis  | —                               | —    | 150  | —    | mV   |
| t <sub>POR</sub>     | Reset delay time  | V <sub>DD</sub> = 3.3 V         | —    | 0.1  | 0.2  | ms   |

Note: 1. Data based on characterization results only, not tested in production.  
2. If the LDO will be turn on, the VDD POR has to be in the de-assertion condition. When the VDD POR is in the assertion state then the LDO will be turn off.

**Table 10. LVD/BOD Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol               | Parameter                        | Conditions   |            | Min. | Typ. | Max. | Unit |
|----------------------|----------------------------------|--|------------|------|------|------|------|
| V <sub>BOD</sub>     | Voltage of Brown Out Detection   | T <sub>A</sub> = -40 °C ~ 85 °C,<br>After factory-trimmed (V <sub>DD</sub> Falling edge) |            | 2.02 | 2.1  | 2.18 | V    |
| V <sub>LVD</sub>     | Voltage of Low Voltage Detection | T <sub>A</sub> = -40 °C ~ 85 °C<br>(V <sub>DD</sub> Falling edge)                        | LVDS = 000 | 2.17 | 2.25 | 2.33 | V    |
|                      |                                  |  | LVDS = 001 | 2.32 | 2.4  | 2.48 | V    |
|                      |                                  |  | LVDS = 010 | 2.47 | 2.55 | 2.63 | V    |
|                      |                                  |  | LVDS = 011 | 2.62 | 2.7  | 2.78 | V    |
|                      |                                  |  | LVDS = 100 | 2.77 | 2.85 | 2.93 | V    |
|                      |                                  |  | LVDS = 101 | 2.92 | 3.0  | 3.08 | V    |
|                      |                                  |  | LVDS = 110 | 3.07 | 3.15 | 3.23 | V    |
|                      |                                  |  | LVDS = 111 | 3.22 | 3.3  | 3.38 | V    |
| V <sub>LVDHTST</sub> | LVD hysteresis                   | V <sub>DD</sub> = 3.3 V  | —          | —    | 100  | —    | mV   |
| t <sub>SULVD</sub>   | LVD Setup time                   | V <sub>DD</sub> = 3.3 V  | —          | —    | —    | 5    | μs   |
| t <sub>ATLVD</sub>   | LVD active delay time            | V <sub>DD</sub> = 3.3 V  | —          | —    | 200  | —    | μs   |
| I <sub>DDLVD</sub>   | Operation current <sup>(2)</sup> | V <sub>DD</sub> = 3.3 V  | —          | —    | 5    | 15   | μA   |

Note: 1. Data based on characterization results only, not tested in production.  
2. Bandgap current is not included.  
3. LVDS field is in PWRCU LVDCSR register.

## External Clock Characteristics

**Table 11. High Speed External Clock (HSE) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol              | Parameter  | Conditions  | Min.   | Typ. | Max. | Unit |
|---------------------|--|---|--------|------|------|------|
| V <sub>DD</sub>     | Operation Range  | —   | 2.0    | —    | 3.6  | V    |
| f <sub>HSE</sub>    | High Speed External oscillator frequency (HSE)             | —   | 4      | —    | 16   | MHz  |
| C <sub>LHSE</sub>   | Load capacitance   | V <sub>DD</sub> = 3.3 V, R <sub>ESR</sub> = 100 Ω @ 16 MHz            | —      | —    | 22   | pF   |
| R <sub>FBHSE</sub>  | Internal feedback resistor between XTALIN and XTALOUT pins | V <sub>DD</sub> = 3.3 V   | —      | 1    | —    | MΩ   |
| R <sub>ESR</sub>    | Equivalent Series Resistance                               | V <sub>DD</sub> = 3.3 V, C <sub>L</sub> = 12 pF @ 16 MHz, HSEGAIN = 0 | —      | —    | 100  | Ω    |
|                     |  | V <sub>DD</sub> = 2.4 V, C <sub>L</sub> = 12 pF @ 16 MHz, HSEGAIN = 1 | —      | —    | 200  |      |
| D <sub>HSE</sub>    | HSE oscillator Duty cycle                                  | —   | 40     | —    | 60   | %    |
| I <sub>DDHSE</sub>  | HSE oscillator current consumption                         | V <sub>DD</sub> = 3.3 V<br>C <sub>L</sub> = 12 pF<br>HSEGAIN = 0      | 8 MHz  | —    | 0.75 | mA   |
|                     |  |   | 16 MHz | —    | 1    |      |
| I <sub>PWDHSE</sub> | HSE oscillator power down current                          | V <sub>DD</sub> = 3.3 V   | —      | —    | 0.01 | μA   |
| t <sub>SUHSE</sub>  | HSE oscillator startup time                                | V <sub>DD</sub> = 3.3 V @ 8 MHz, HSEGAIN = 0                          | —      | —    | 4    | ms   |

**Table 12. Low Speed External Clock (LSE) Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol              | Parameter                                     | Conditions   | Min. | Typ.   | Max. | Unit |
|---------------------|---|--|------|--------|------|------|
| V <sub>BAK</sub>    | Operation Range                               | —  | 2.0  | —      | 3.6  | V    |
| f <sub>CK_LSE</sub> | Frequency of LSE                              | V <sub>BAK</sub> = 2.0 V ~ 3.6 V   | —    | 32.768 | —    | kHz  |
| R <sub>F</sub>      | Internal feedback resistor                    | —  | —    | 10     | —    | MΩ   |
| R <sub>ESR</sub>    | Equivalent Series Resistance                  | V <sub>BAK</sub> = 3.3 V   | 30   | —      | TBD  | kΩ   |
| C <sub>L</sub>      | Recommended load capacitances                 | V <sub>BAK</sub> = 3.3 V   | 6    | —      | TBD  | pF   |
| I <sub>DDLSE</sub>  | Oscillator supply current (High current mode) | f <sub>CK_LSE</sub> = 32.768 kHz, R <sub>ESR</sub> = 50 kΩ, C <sub>L</sub> ≥ 7 pF, V <sub>BAK</sub> = 2.0V ~ 2.7 V, T <sub>A</sub> = -40 °C ~ 85 °C  | —    | 3.3    | 6.3  | μA   |
|                     | Oscillator supply current (Low current mode)  | f <sub>CK_LSE</sub> = 32.768 kHz, R <sub>ESR</sub> = 50 kΩ, C <sub>L</sub> < 7 pF, V <sub>BAK</sub> = 2.0 V ~ 3.6 V, T <sub>A</sub> = -40 °C ~ 85 °C | —    | 1.8    | 3.3  | μA   |
|                     | Power down current                            | —  | —    | —      | 0.01 | μA   |
| t <sub>SULSE</sub>  | Startup time (Low current mode)               | f <sub>CK_LSE</sub> = 32.768 kHz, V <sub>BAK</sub> = 2.7 V ~ 3.6 V   | —    | 2.5    | —    | s    |

Note: The following guidelines are recommended to increase the robustness of the crystal circuit of the HSE / LSE clock in the PCB layout phase.

1. The crystal oscillator should be located as close as possible to the MCU so that the trace length would be as short as possible to reduce the parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep the frequently switching signal lines away from the crystal area to prevent the crosstalk.



## Internal Clock Characteristics

**Table 13. High Speed Internal Clock (HSI) Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol      | Parameter   | Conditions   | Min. | Typ. | Max. | Unit          |
|-------------|---|--|------|------|------|---------------|
| $V_{DD}$    | Operation Range   | —  | 2.0  | —    | 3.6  | V             |
| $f_{HSI}$   | Frequency of HSI  | $V_{DD} = 3.3\text{ V @ }25\text{ }^{\circ}\text{C}$   | —    | 8    | —    | MHz           |
| $ACC_{HSI}$ | Frequency accuracy of the factory-calibrated HSI oscillator | $V_{DD} = 3.3\text{ V}, T_A = 25\text{ }^{\circ}\text{C}$  | -2   | —    | 2    | %             |
|             |   | $V_{DD} = 2.5\text{ V} \sim 3.6\text{ V}, T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | -3   | —    | 3    | %             |
|             |   | $V_{DD} = 2.0\text{ V} \sim 3.6\text{ V}, T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | -4   | —    | 4    | %             |
| Duty        | Duty cycle  | $f_{HSI} = 8\text{ MHz}$   | 35   | —    | 65   | %             |
| $I_{DDHSI}$ | Oscillator supply current                                   | $f_{HSI} = 8\text{ MHz}$   | —    | 220  | 250  | $\mu\text{A}$ |
|             | Power down current  |  | —    | —    | 0.05 | $\mu\text{A}$ |
| $t_{SUHSI}$ | Startup time  | $f_{HSI} = 8\text{ MHz}$   | —    | —    | 10   | $\mu\text{s}$ |

**Table 14. Low Speed Internal Clock (LSI) Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol       | Parameter                                     | Conditions  | Min. | Typ. | Max. | Unit          |
|--------------|---|---|------|------|------|---------------|
| $f_{LSI}$    | Low Speed Internal Oscillator Frequency (LSI) | $V_{BAK} = 3.3\text{ V}, T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | 21   | 32   | 43   | kHz           |
| $ACC_{LSI}$  | Frequency accuracy of LSI                     | After factory-trimmed, $V_{BAK} = 3.3\text{ V}, T_A = 25\text{ }^{\circ}\text{C}$           | -10  | —    | +10  | %             |
| $I_{DDL SI}$ | LSI Oscillator Operating current              | $V_{BAK} = 3.3\text{ V}, T_A = 25\text{ }^{\circ}\text{C}$                                  | —    | 0.8  | 1.2  | $\mu\text{A}$ |
| $t_{SULSI}$  | LSI Oscillator startup time                   | $V_{BAK} = 3.3\text{ V}, T_A = 25\text{ }^{\circ}\text{C}$                                  | —    | —    | 100  | $\mu\text{s}$ |

## PLL Characteristics

**Table 15. PLL Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol        | Parameter        | Conditions | Min. | Typ. | Max. | Unit          |
|---------------|------------------|------------|------|------|------|---------------|
| $f_{PLLIN}$   | PLL input clock  | —          | 4    | —    | 16   | MHz           |
| $f_{CK\_PLL}$ | PLL output clock | —          | 64   | —    | 96   | MHz           |
| $t_{LOCK}$    | PLL lock time    | —          | —    | 200  | —    | $\mu\text{s}$ |

## USB PLL Characteristics

**Table 16. USB PLL Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol        | Parameter        | Conditions | Min. | Typ. | Max. | Unit          |
|---------------|------------------|------------|------|------|------|---------------|
| $f_{PLLIN}$   | PLL input clock  | —          | 4    | —    | 16   | MHz           |
| $f_{CK\_PLL}$ | PLL output clock | —          | 16   | —    | 48   | MHz           |
| $t_{LOCK}$    | PLL lock time    | —          | —    | 200  | —    | $\mu\text{s}$ |

## Memory Characteristics

**Table 17. Flash Memory Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol              | Parameter  | Conditions  | Min. | Typ. | Max. | Unit          |
|---------------------|--|---|------|------|------|---------------|
| $N_{\text{ENDU}}$   | Number of guaranteed program/erase cycles before failure (Endurance) | $T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | 20   | —    | —    | K cycles      |
| $t_{\text{RET}}$    | Data retention time  | $T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | 10   | —    | —    | Years         |
| $t_{\text{PROG}}$   | Word programming time  | $T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | 20   | —    | —    | $\mu\text{s}$ |
| $t_{\text{ERASE}}$  | Page erase time  | $T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | 2    | —    | —    | ms            |
| $t_{\text{MERASE}}$ | Mass erase time  | $T_A = -40\text{ }^{\circ}\text{C} \sim 85\text{ }^{\circ}\text{C}$ | 10   | —    | —    | ms            |

## I/O Port Characteristics

**Table 18. I/O Port Characteristics**

$T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

| Symbol           | Parameter                                       | Conditions  | Min.                 | Typ.                 | Max.                  | Unit          |
|------------------|---|---|----------------------|----------------------|-----------------------|---------------|
| $I_{\text{IL}}$  | Low level input current                         | 3.3 V I/O   | —                    | —                    | 3                     | $\mu\text{A}$ |
|                  |   | Reset pin   | —                    | —                    | 3                     | $\mu\text{A}$ |
| $I_{\text{IH}}$  | High level input current                        | 3.3 V I/O   | —                    | —                    | 3                     | $\mu\text{A}$ |
|                  |   | Reset pin   | —                    | —                    | 3                     | $\mu\text{A}$ |
| $V_{\text{IL}}$  | Low level input voltage                         | 3.3 V I/O   | -0.5                 | —                    | 0.35 $V_{\text{DD}}$  | V             |
|                  |   | Reset pin   | -0.5                 | —                    | 0.35 $V_{\text{DD}}$  | V             |
| $V_{\text{IH}}$  | High level input voltage                        | 3.3 V I/O   | 0.65 $V_{\text{DD}}$ | —                    | $V_{\text{DD}} + 0.5$ | V             |
|                  |   | Reset pin   | 0.65 $V_{\text{DD}}$ | —                    | $V_{\text{DD}} + 0.5$ | V             |
| $V_{\text{HYS}}$ | Schmitt trigger input voltage hysteresis        | 3.3 V I/O   | —                    | 0.12 $V_{\text{DD}}$ | —                     | mV            |
|                  |   | Reset pin   | —                    | 0.12 $V_{\text{DD}}$ | —                     | mV            |
| $I_{\text{OL}}$  | Low level output current (GPIO Sink current)    | 3.3 V I/O 4 mA drive, $V_{\text{OL}} = 0.4\text{ V}$  | 4                    | —                    | —                     | mA            |
|                  |   | 3.3 V I/O 8 mA drive, $V_{\text{OL}} = 0.4\text{ V}$  | 8                    | —                    | —                     | mA            |
|                  |   | 3.3 V I/O 12 mA drive, $V_{\text{OL}} = 0.4\text{ V}$   | 12                   | —                    | —                     | mA            |
|                  |   | 3.3 V I/O 16 mA drive, $V_{\text{OL}} = 0.4\text{ V}$   | 16                   | —                    | —                     | mA            |
|                  |   | Backup Domain I/O drive @ $V_{\text{DD}} = 3.3\text{ V}$ , $V_{\text{OL}} = 0.4\text{ V}$ , PB10, PB11, PB12                  | 4                    | —                    | —                     | mA            |
| $I_{\text{OH}}$  | High level output current (GPIO Source current) | 3.3 V I/O 4 mA drive, $V_{\text{OH}} = V_{\text{DD}} - 0.4\text{ V}$  | 4                    | —                    | —                     | mA            |
|                  |   | 3.3 V I/O 8 mA drive, $V_{\text{OH}} = V_{\text{DD}} - 0.4\text{ V}$  | 8                    | —                    | —                     | mA            |
|                  |   | 3.3 V I/O 12 mA drive, $V_{\text{OH}} = V_{\text{DD}} - 0.4\text{ V}$   | 12                   | —                    | —                     | mA            |
|                  |   | 3.3 V I/O 16 mA drive, $V_{\text{OH}} = V_{\text{DD}} - 0.4\text{ V}$   | 16                   | —                    | —                     | mA            |
|                  |   | Backup Domain I/O drive @ $V_{\text{DD}} = 3.3\text{ V}$ , $V_{\text{OL}} = V_{\text{DD}} - 0.4\text{ V}$ , PB10, PB11, PB12. | —                    | —                    | 2                     | mA            |

| Symbol          | Parameter                   | Conditions  | Min.                            | Typ.                  | Max. | Unit |   |
|-----------------|-----------------------------|---|---------------------------------|-----------------------|------|------|---|
| V <sub>OL</sub> | Low level output voltage    | 3.3 V 4 mA drive I/O, I <sub>OL</sub> = 4 mA                  | —                               | —                     | 0.4  | V    |   |
|                 |                             | 3.3 V 8 mA drive I/O, I <sub>OL</sub> = 8 mA                  | —                               | —                     | 0.4  | V    |   |
|                 |                             | 3.3 V 12 mA drive I/O, I <sub>OL</sub> = 12 mA                | —                               | —                     | 0.4  | V    |   |
|                 |                             | 3.3 V 16 mA drive I/O, I <sub>OL</sub> = 16 mA                | —                               | —                     | 0.4  | V    |   |
|                 |                             | Backup Domain I/O Sink Current = 4 mA (Low driving strength)  | V <sub>DD</sub> = 2.7 V ~ 3.6 V | —                     | —    | 0.4  | V |
|                 |                             |   | V <sub>DD</sub> = 2.0 V ~ 2.7 V | —                     | —    | 0.6  | V |
|                 |                             | Backup Domain I/O Sink Current = 8 mA (High driving strength) | V <sub>DD</sub> = 2.7 V ~ 3.6 V | —                     | —    | 0.4  | V |
|                 |                             |   | V <sub>DD</sub> = 2.0 V ~ 2.7 V | —                     | —    | 0.6  | V |
| V <sub>OH</sub> | High level output voltage   | 3.3 V 4 mA drive I/O, I <sub>OH</sub> = 4 mA                  | V <sub>DD</sub> - 0.4           | —                     | —    | V    |   |
|                 |                             | 3.3 V 8 mA drive I/O, I <sub>OH</sub> = 8 mA                  | V <sub>DD</sub> - 0.4           | —                     | —    | V    |   |
|                 |                             | 3.3 V 12 mA drive I/O, I <sub>OL</sub> = 12 mA                | V <sub>DD</sub> - 0.4           | —                     | —    | V    |   |
|                 |                             | 3.3 V 16 mA drive I/O, I <sub>OL</sub> = 16 mA                | V <sub>DD</sub> - 0.4           | —                     | —    | V    |   |
|                 |                             | Backup Domain I/O Source Current = 2 mA                       | V <sub>DD</sub> = 2.7 V ~ 3.6 V | 2.4                   | —    | —    | V |
|                 |                             | Backup Domain I/O Source Current = 1 mA                       | V <sub>DD</sub> = 2.0 V ~ 2.7 V | V <sub>DD</sub> - 0.4 | —    | —    | V |
| R <sub>PU</sub> | Internal pull-up resistor   | 3.3 V I/O   | —                               | 46                    | —    | kΩ   |   |
| R <sub>PD</sub> | Internal pull-down resistor | 3.3 V I/O   | —                               | 46                    | —    | kΩ   |   |

## ADC Characteristics

Table 19. ADC Characteristics

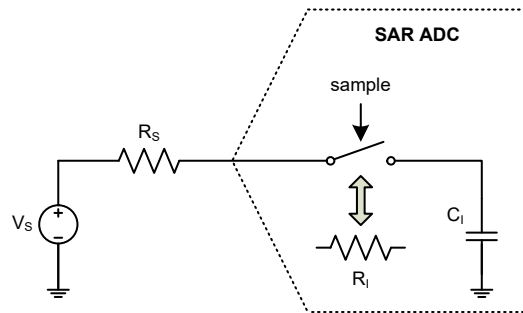
T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol               | Parameter                         | Conditions                      | Min. | Typ.             | Max.              | Unit                         |
|----------------------|-----------------------------------|---------------------------------|------|------------------|-------------------|------------------------------|
| V <sub>DDA</sub>     | Operating voltage                 | —                               | 2.5  | 3.3              | 3.6               | V                            |
| V <sub>ADCIN</sub>   | A/D Converter input voltage range | —                               | 0    | —                | V <sub>REF+</sub> | V                            |
| V <sub>REF+</sub>    | A/D Converter Reference voltage   | —                               | —    | V <sub>DDA</sub> | V <sub>DDA</sub>  | V                            |
| I <sub>ADC</sub>     | Current consumption               | V <sub>DDA</sub> = 3.3 V        | —    | 0.85             | 1                 | mA                           |
| I <sub>ADC_DN</sub>  | Power down current consumption    | V <sub>DDA</sub> = 3.3 V        | —    | —                | 0.1               | μA                           |
| f <sub>ADC</sub>     | A/D Converter clock               | —                               | 0.7  | —                | 16                | MHz                          |
| f <sub>s</sub>       | Sampling rate                     | —                               | 0.05 | —                | 1                 | MHz                          |
| t <sub>DL</sub>      | Data latency                      | —                               | —    | 12.5             | —                 | 1/f <sub>ADC</sub><br>Cycles |
| t <sub>s&amp;H</sub> | Sampling & hold time              | —                               | —    | 3.5              | —                 | 1/f <sub>ADC</sub><br>Cycles |
| t <sub>ADCCONV</sub> | A/D Converter conversion time     | ADST[7:0] = 2                   | —    | 16               | —                 | 1/f <sub>ADC</sub><br>Cycles |
| R <sub>i</sub>       | Input sampling switch resistance  | —                               | —    | —                | 1                 | kΩ                           |
| C <sub>i</sub>       | Input sampling capacitance        | No pin/pad capacitance included | —    | 16               | —                 | pF                           |
| t <sub>SU</sub>      | Startup time                      | —                               | —    | —                | 1                 | μs                           |
| N                    | Resolution                        | —                               | —    | 12               | —                 | bits                         |

| Symbol | Parameter                        | Conditions                                       | Min. | Typ.    | Max.     | Unit |
|--------|----------------------------------|--|------|---------|----------|------|
| INL    | Integral Non-linearity error     | $f_s = 750 \text{ kHz}, V_{DDA} = 3.3 \text{ V}$ | —    | $\pm 2$ | $\pm 5$  | LSB  |
| DNL    | Differential Non-linearity error | $f_s = 750 \text{ kHz}, V_{DDA} = 3.3 \text{ V}$ | —    | $\pm 1$ | —        | LSB  |
| $E_o$  | Offset error                     | —  | —    | —       | $\pm 10$ | LSB  |
| $E_G$  | Gain error                       | —  | —    | —       | $\pm 10$ | LSB  |

Note: 1. Data based on characterization results only, not tested in production.

- Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the  $V_{DDA}$  supply power of the A/D Converter has to be equal to the  $V_{DD}$  supply power of the MCU in the application circuit.
- The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where  $C_i$  is the storage capacitor,  $R_i$  is the resistance of the sampling switch and  $R_s$  is the output impedance of the signal source  $V_s$ . Normally the sampling phase duration is approximately,  $3.5/f_{ADC}$ . The capacitance,  $C_i$ , must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to  $V_s$  for accuracy. To guarantee this,  $R_s$  may not have an arbitrarily large value.



**Figure 6. Figure 7 ADC Sampling Network Model**

The worst case occurs when the extremities of the input range (0V and  $V_{REF}$ ) are sampled consecutively. In this situation a sampling error below  $\frac{1}{4}$  LSB is ensured by using the following equation:

$$R_s < \frac{3.5}{f_{ADC} C_i \ln(2^{N+2})} - R_i$$

Where  $f_{ADC}$  is the ADC clock frequency and  $N$  is the ADC resolution ( $N = 12$  in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases,  $R_s$  may be larger than the value indicated by the equation above.

## Comparator Characteristics

**Table 20. Comparator Characteristics**

T<sub>A</sub> = 25 °C, unless otherwise specified.

| Symbol                                    | Parameter                                       | Conditions   | Min.                     | Typ. | Max.             | Unit |
|---|---|--|--------------------------|------|------------------|------|
| V <sub>DDA</sub>                          | Operating voltage                               | Comparator mode  | 2.5                      | 3.3  | 3.6              | V    |
| V <sub>IN</sub>                           | Input Common Mode Voltage Range                 | CP or CN   | V <sub>SSA</sub>         | —    | V <sub>DDA</sub> | V    |
| V <sub>IOS</sub>                          | Input offset voltage <sup>(1)</sup>             | T <sub>A</sub> = 25 °C                                       | -15                      | —    | 15               | mV   |
| V <sub>HYS</sub>                          | Input Hysteresis                                | No hysteresis (CMPnHM[1:0] = 00)                             | Low Speed                | —    | 0                | —    |
|   |   |  | High Speed               | —    | 0                | —    |
|   |   | Low hysteresis (CMPnHM[1:0] = 01)                            | Low Speed                | —    | 30               | —    |
|   |   |  | High Speed               | —    | 30               | —    |
|   |   | Middle hysteresis (CMPnHM[1:0] = 10)                         | Low Speed                | —    | 50               | —    |
|   |   |  | High Speed               | —    | 70               | —    |
|   |   | High hysteresis (CMPnHM[1:0] = 11)                           | Low Speed                | —    | 70               | —    |
|   |   |  | High Speed               | —    | 100              | —    |
| t <sub>RT</sub>                           | Response time<br>Input Overdrive = ±100mV       | High Speed mode  | V <sub>DDA</sub> ≥ 2.7 V | —    | 50               | 100  |
|   |   |  | V <sub>DDA</sub> < 2.7 V | —    | 100              | 250  |
|   |   | Low Speed mode   | —                        | 2    | 5                | —    |
| I <sub>CMP</sub>                          | Current Consumption<br>V <sub>DDA</sub> = 3.3 V | High Speed mode  | —                        | 180  | —                | —    |
|   |   | Low Speed mode   | —                        | 30   | —                | —    |
| t <sub>CMPST</sub>                        | Comparator Startup Time                         | Comparator enabled to output valid                           | —                        | —    | 50               | —    |
| I <sub>CMP_DN</sub>                       | Power Down Supply Current                       | CMPEN = 0, CVREN = 0<br>CVROE = 0                            | —                        | —    | 0.1              | —    |
| <b>Comparator Voltage Reference (CVR)</b> |   |  |                          |      |                  |      |
| V <sub>CVR</sub>                          | Output Range                                    | —  | V <sub>SSA</sub>         | —    | V <sub>DDA</sub> | V    |
| N <sub>Bits</sub>                         | CVR Scaler Resolution                           | —  | —                        | 6    | —                | bits |
| t <sub>CVRST</sub>                        | Setting Time                                    | CVR scaler setting time from<br>CVREF = "000000" to "111111" | —                        | —    | 100              | —    |
| I <sub>CVR</sub>                          | Current Consumption<br>V <sub>DDA</sub> = 3.3 V | CVREN = 1, CMPREFOE = 0                                      | —                        | 65   | —                | —    |
|   |   | CVREN = 1, CVROE = 1   | —                        | 80   | 110              | —    |

Note: Data based on characterization results only, not tested in production.

## GPTM/MCTM Characteristics

**Table 21. GPTM/MCTM Characteristics**

| Symbol           | Parameter                                  | Conditions | Min. | Typ. | Max. | Unit              |
|------------------|--|------------|------|------|------|-------------------|
| f <sub>TM</sub>  | Timer clock source for GPTM and MCTM       | —          | —    | —    | 96   | MHz               |
| t <sub>RES</sub> | Timer resolution time                      | —          | 1    | —    | —    | 1/f <sub>TM</sub> |
| f <sub>EXT</sub> | External single frequency on channel 1 ~ 4 | —          | —    | —    | 1/2  | f <sub>TM</sub>   |
| RES              | Timer resolution                           | —          | —    | —    | 16   | bits              |

## I<sup>2</sup>C Characteristics

**Table 22. I<sup>2</sup>C Characteristics**

| Symbol               | Parameter                         | Standard Mode |      | Fast Mode |       | Fast Mode Plus |       | Unit |
|----------------------|-----------------------------------|---------------|------|-----------|-------|----------------|-------|------|
|                      |                                   | Min.          | Max. | Min.      | Max.  | Min.           | Max.  |      |
| f <sub>SCL</sub>     | SCL clock frequency               | —             | 100  | —         | 400   | —              | 1000  | kHz  |
| t <sub>SCL(H)</sub>  | SCL clock high time               | 4.5           | —    | 1.125     | —     | 0.45           | —     | μs   |
| t <sub>SCL(L)</sub>  | SCL clock low time                | 4.5           | —    | 1.125     | —     | 0.45           | —     | μs   |
| t <sub>FALL</sub>    | SCL and SDA fall time             | —             | 1.3  | —         | 0.34  | —              | 0.135 | μs   |
| t <sub>RISE</sub>    | SCL and SDA rise time             | —             | 1.3  | —         | 0.34  | —              | 0.135 | μs   |
| t <sub>SU(SDA)</sub> | SDA data setup time               | 500           | —    | 125       | —     | 50             | —     | ns   |
| t <sub>H(SDA)</sub>  | SDA data hold time <sup>(5)</sup> | 0             | —    | 0         | —     | 0              | —     | ns   |
|                      | SDA data hold time <sup>(6)</sup> | 100           | —    | 100       | —     | 100            | —     | ns   |
| t <sub>VD(SDA)</sub> | SDA data valid time               | —             | 1.6  | —         | 0.475 | —              | 0.25  | μs   |
| t <sub>SU(STA)</sub> | START condition setup time        | 500           | —    | 125       | —     | 50             | —     | ns   |
| t <sub>H(STA)</sub>  | START condition hold time         | 0             | —    | 0         | —     | 0              | —     | ns   |
| t <sub>SU(STO)</sub> | STOP condition setup time         | 500           | —    | 125       | —     | 50             | —     | ns   |

Note: 1. Data based on characterization results only, not tested in production.

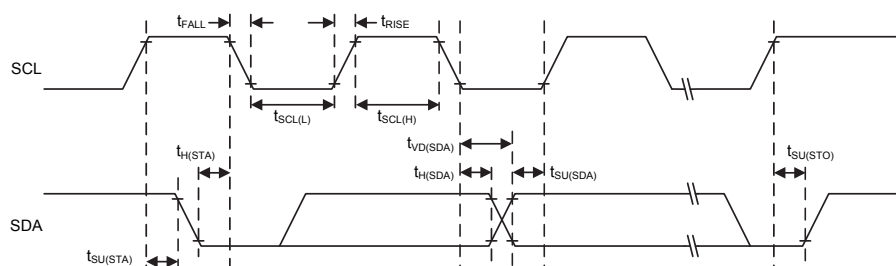
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.

3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.

4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.

5. The above characteristic parameters of the I<sup>2</sup>C bus timing are based on: COMB\_FILTER\_En = 0 and SEQ\_FILTER = 00.

6. The above characteristic parameters of the I<sup>2</sup>C bus timing are based on: COMB\_FILTER\_En = 1 and SEQ\_FILTER = 00.



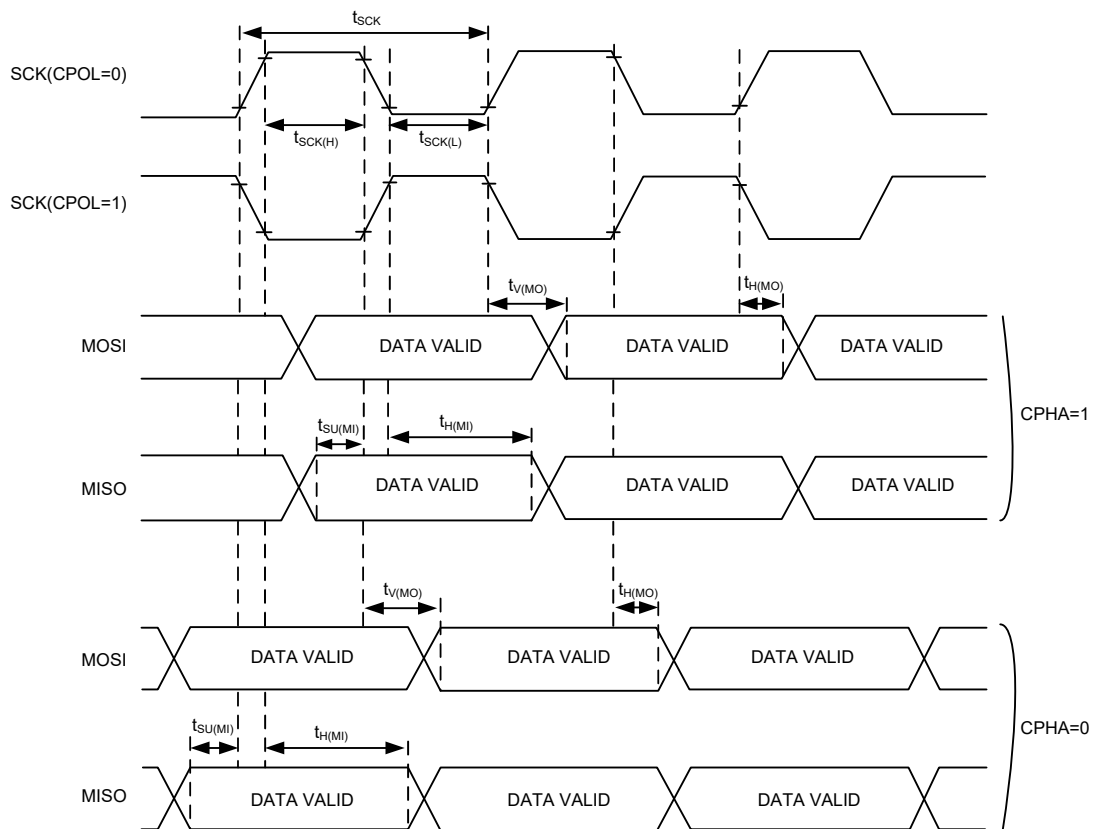
**Figure 7. I<sup>2</sup>C Timing Diagrams**

## SPI Characteristics

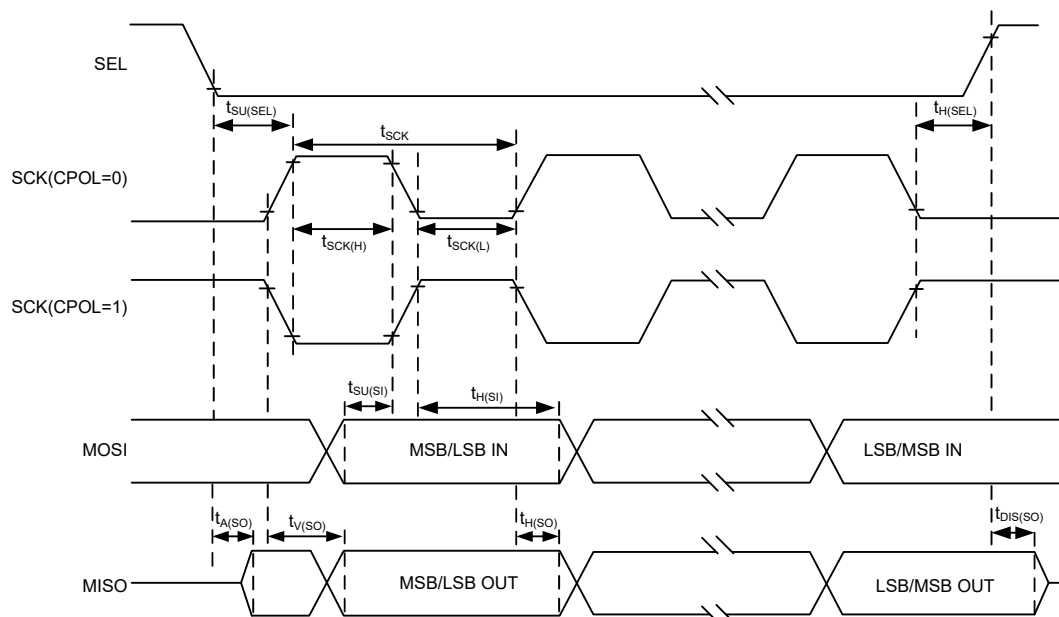
**Table 23. SPI Characteristics**

| Symbol                       | Parameter                             | Conditions   | Min.                | Typ. | Max.                | Unit |
|------------------------------|---------------------------------------|--|---------------------|------|---------------------|------|
| <b>SPI Master mode</b>       |                                       |  |                     |      |                     |      |
| $f_{SCK}$ (1/ $t_{SCK}$ )    | SPI master output SCK clock frequency | Master mode<br>SPI peripheral clock frequency $f_{PCLK}$ | —                   | —    | $f_{PCLK}/2$        | MHz  |
| $t_{SCK(H)}$<br>$t_{SCK(L)}$ | SCK clock high and low time           | —  | $t_{SCK}/2 - 2$     | —    | $t_{SCK}/2 + 1$     | ns   |
| $t_{V(MO)}$                  | Data output valid time                | —  | —                   | —    | 5                   | ns   |
| $t_{H(MO)}$                  | Data output hold time                 | —  | 2                   | —    | —                   | ns   |
| $t_{SU(MI)}$                 | Data input setup time                 | —  | 5                   | —    | —                   | ns   |
| $t_{H(MI)}$                  | Data input hold time                  | —  | 5                   | —    | —                   | ns   |
| <b>SPI Slave mode</b>        |                                       |  |                     |      |                     |      |
| $f_{SCK}$ (1/ $t_{SCK}$ )    | SPI slave input SCK clock frequency   | Slave mode<br>SPI peripheral clock frequency $f_{PCLK}$  | —                   | —    | $f_{PCLK}/3$        | MHz  |
| Duty <sub>SCK</sub>          | SPI slave input SCK clock duty cycle  | —  | 30                  | —    | 70                  | %    |
| $t_{SU(SEL)}$                | SEL enable setup time                 | —  | $3 \times t_{PCLK}$ | —    | —                   | ns   |
| $t_{H(SEL)}$                 | SEL enable hold time                  | —  | $2 \times t_{PCLK}$ | —    | —                   | ns   |
| $t_{A(SO)}$                  | Data output access time               | —  | —                   | —    | $3 \times t_{PCLK}$ | ns   |
| $t_{DIS(SO)}$                | Data output disable time              | —  | —                   | —    | 10                  | ns   |
| $t_{V(SO)}$                  | Data output valid time                | —  | —                   | —    | 25                  | ns   |
| $t_{H(SO)}$                  | Data output hold time                 | —  | 15                  | —    | —                   | ns   |
| $t_{SU(SI)}$                 | Data input setup time                 | —  | 5                   | —    | —                   | ns   |
| $t_{H(SI)}$                  | Data input hold time                  | —  | 4                   | —    | —                   | ns   |

Note:  $t_{SCK} = 1/f_{SCK}$ ;  $t_{PCLK} = 1/f_{PCLK}$ . SPI output (input) clock frequency  $f_{SCK}$ ; SPI peripheral clock frequency  $f_{PCLK}$ .



**Figure 8. SPI Timing Diagrams – SPI Master Mode**



**Figure 9. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1**



## I<sup>2</sup>S Characteristics

**Table 24. I<sup>2</sup>S Characteristics**

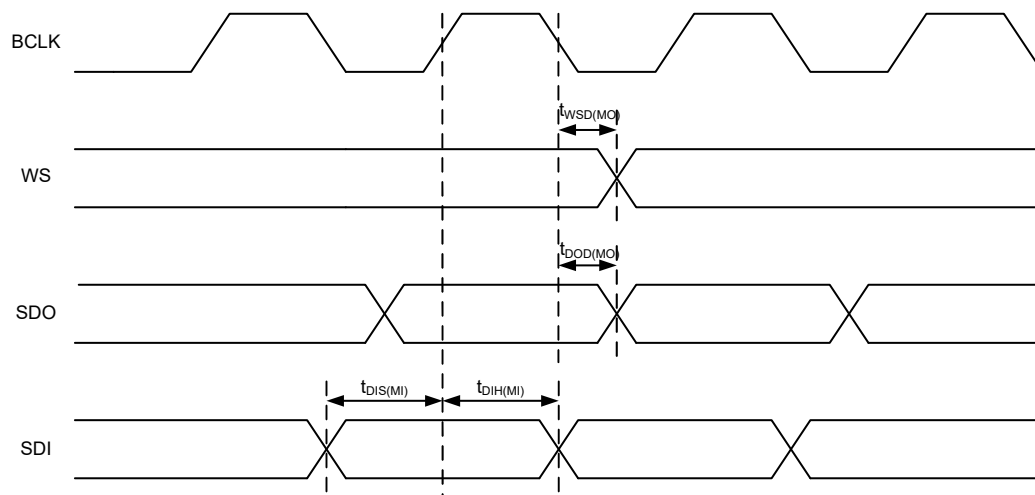
| Symbol                            | Parameter                 | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|---------------------------|------------|------|------|------|------|
| <b>I<sup>2</sup>S Master mode</b> |                           |            |      |      |      |      |
| $t_{WSD(MO)}$                     | WS output to BCLK delay   | —          | 0    | —    | 4.6  | ns   |
| $t_{DOD(MO)}$                     | Data output to BCLK delay | —          | 0.5  | —    | 5.4  | ns   |
| $t_{DIS(MI)}$                     | Data input setup time     | —          | 0    | —    | —    | ns   |
| $t_{DIH(MI)}$                     | Data input hold time      | —          | 13   | —    | —    | ns   |
| <b>I<sup>2</sup>S Slave mode</b>  |                           |            |      |      |      |      |
| $t_{BCH(SI)}$                     | BCLK high pulse width     | —          | 42   | —    | —    | ns   |
| $t_{BCL(SI)}$                     | BCLK low pulse width      | —          | 42   | —    | —    | ns   |
| $t_{WSS(SI)}$                     | WS input setup time       | —          | 0    | —    | —    | ns   |
| $t_{DOD(SO)}$                     | Data output to BCLK delay | —          | —    | —    | 9    | ns   |
| $t_{DIS(SI)}$                     | Data input setup time     | —          | 0    | —    | —    | ns   |
| $t_{DIH(SI)}$                     | Data input hold time      | —          | 2.1  | —    | —    | ns   |

Note: 1. Data based on characterization results only, not tested in production. Data based on characterization results only, not tested in production.

2. I/O driving current is set to 4 mA.

3. Capacitive load  $C = 10$  pF,  $V_{DD} = 3.3$  V and ambient temperature  $T_A = 25$  °C.

4. Measurement points are set at CMOS levels = 0.5  $V_{DD}$ .



**Figure 10. Timing of I<sup>2</sup>S Master Mode**

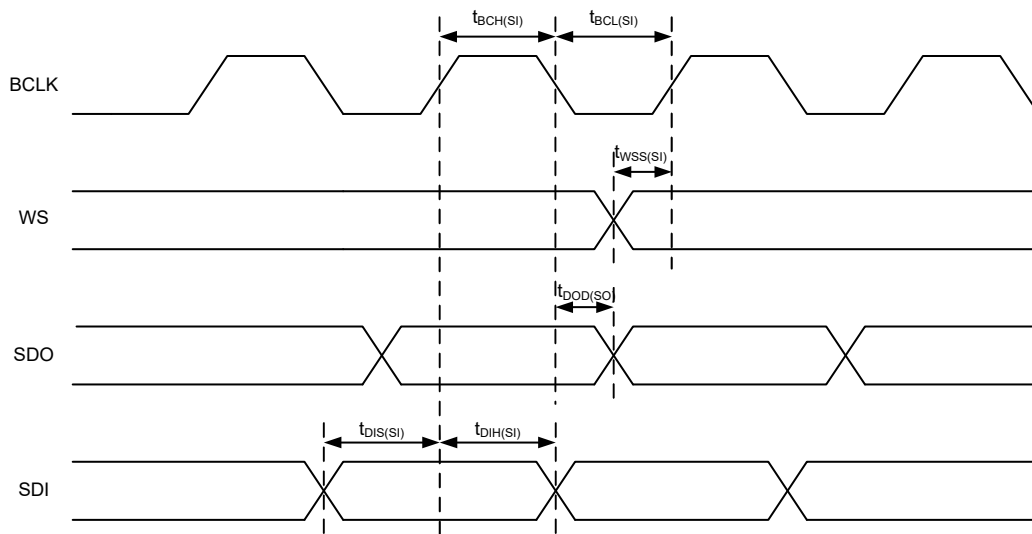


Figure 11. Timing of I²S Slave Mode

## SDIO Characteristics

Table 25. SDIO Characteristics

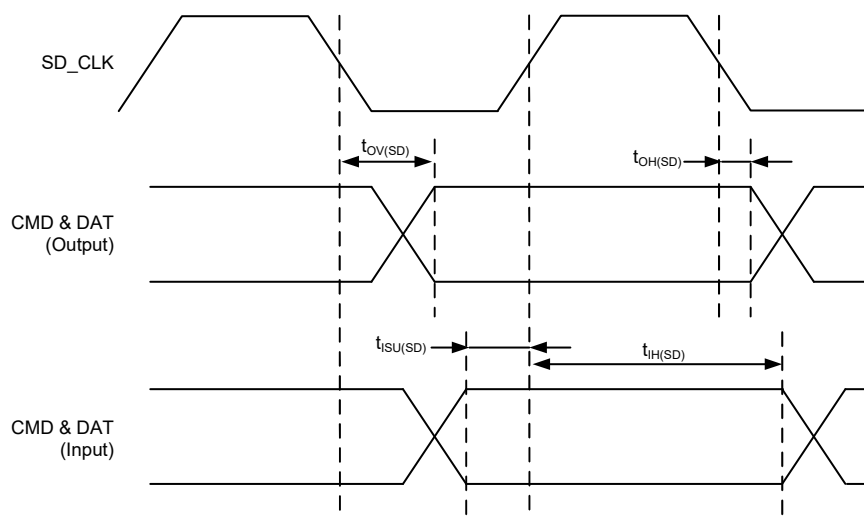
| Symbol   | Parameter                             | Conditions                  | Min. | Typ. | Max. | Unit |
|--|---------------------------------------|-----------------------------|------|------|------|------|
| $f_{SDCK}$   | Clock frequency in data transfer mode | —                           | —    | —    | 48   | MHz  |
| $t_{W(CKL)}$   | Clock low time                        | $f_{SDCK} = 48 \text{ MHz}$ | —    | 9    | —    | ns   |
| $t_{W(CKH)}$   | Clock high time                       | $f_{SDCK} = 48 \text{ MHz}$ | —    | 10   | —    | ns   |
| <b>CMD, Data inputs referenced to SD_CLK in SD default mode</b>  |                                       |                             |      |      |      |      |
| $t_{SU(SD)}$   | Input setup time SD default mode      | $f_{SDCK} = 24 \text{ MHz}$ | 3    | —    | —    | ns   |
| $t_{IH(SD)}$   | Input hold time SD default mode       | $f_{SDCK} = 24 \text{ MHz}$ | 0    | —    | —    | ns   |
| <b>CMD, Data outputs referenced to SD_CLK in SD default mode</b> |                                       |                             |      |      |      |      |
| $t_{OV(SD)}$   | Output valid time SD default mode     | $f_{SDCK} = 24 \text{ MHz}$ | —    | 5    | 7    | ns   |
| $t_{OH(SD)}$   | Output hold time SD default mode      | $f_{SDCK} = 24 \text{ MHz}$ | 2    | —    | —    | ns   |
| <b>CMD, Data inputs referenced to SD_CLK in SD HS mode</b>       |                                       |                             |      |      |      |      |
| $t_{SU(HS)}$   | Input setup time SD HS mode           | $f_{SDCK} = 48 \text{ MHz}$ | 2    | —    | —    | ns   |
| $t_{IH(HS)}$   | Input hold time SD HS mode            | $f_{SDCK} = 48 \text{ MHz}$ | 0.5  | —    | —    | ns   |
| <b>CMD, Data outputs referenced to SD_CLK in SD HS mode</b>      |                                       |                             |      |      |      |      |
| $t_{OV(HS)}$   | Output valid time SD HS mode          | $f_{SDCK} = 48 \text{ MHz}$ | —    | 6.5  | 8    | ns   |
| $t_{OH(HS)}$   | Output hold time SD HS mode           | $f_{SDCK} = 48 \text{ MHz}$ | 1.5  | —    | —    | ns   |

Note: 1. Data based on characterization results only, not tested in production.

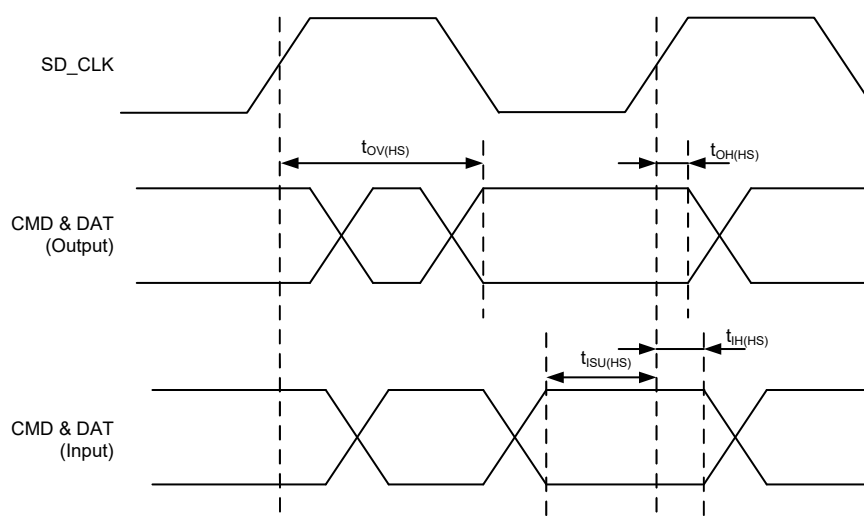
2. I/O driving current is set to 16 mA.

3. Capacitive load  $C = 30 \text{ pF}$ ,  $V_{DD} = 3.3 \text{ V}$  and ambient temperature  $T_A = 25^\circ\text{C}$ .

4. Measurement points are set at CMOS levels =  $0.5 V_{DD}$ .



**Figure 12. SDIO Default Mode**



**Figure 13. SDIO High-speed Mode**

## USB Characteristics

The USB interface is USB-IF certified – Full Speed.

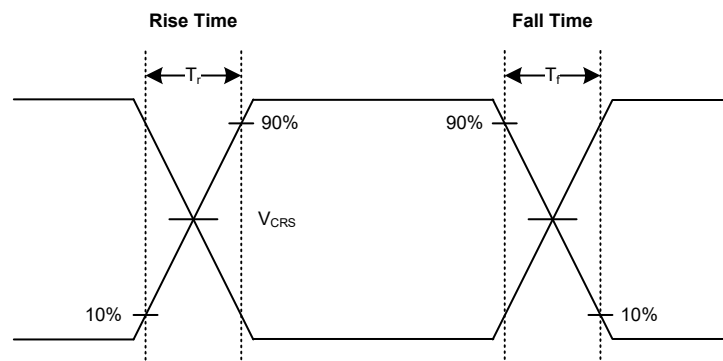
**Table 26. USB DC Electrical Characteristics**

| Symbol    | Parameter                                      | Conditions                          | Min. | Typ. | Max. | Unit     |
|-----------|--|-------------------------------------|------|------|------|----------|
| $V_{DD}$  | USB operating voltage                          | —                                   | 3.0  | —    | 3.6  | V        |
| $V_{DI}$  | Differential input sensitivity                 | USBDP – USBDM                       | 0.2  | —    | —    | V        |
| $V_{CM}$  | Common mode voltage range                      | —                                   | 0.8  | —    | 2.5  | V        |
| $V_{SE}$  | Single-ended receiver threshold                | —                                   | 0.8  | —    | 2.0  | V        |
| $V_{OL}$  | Pad output low voltage                         | $R_L$ of 1.5 k $\Omega$ to $V_{DD}$ | 0    | —    | 0.3  | V        |
| $V_{OH}$  | Pad output high voltage                        |                                     | 2.8  | —    | 3.6  | V        |
| $V_{CRS}$ | Differential output signal cross-point voltage |                                     | 1.3  | —    | 2.0  | V        |
| $Z_{DRV}$ | Driver output resistance                       | —                                   | —    | 10   | —    | $\Omega$ |
| $C_{IN}$  | Transceiver pad capacitance                    | —                                   | —    | —    | 20   | pF       |

Note: 1. Data based on characterization results only, not tested in production.

2. The USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which will experience degradation in the 2.7 V to 3.0 V voltage range.

3.  $R_L$  is the internal resistor load connected to the USB driver USBDP.



**Figure 14. USB Signal Rise Time and Fall Time and Cross-Point Voltage ( $V_{CRS}$ ) Definition**

**Table 27. USB AC Electrical Characteristics**

| Symbol    | Parameter                      | Conditions            | Min. | Typ. | Max. | Unit |
|-----------|--------------------------------|-----------------------|------|------|------|------|
| $t_r$     | Rise time                      | $C_L = 50$ pF         | 4    | —    | 20   | ns   |
| $t_f$     | Fall time                      | $C_L = 50$ pF         | 4    | —    | 20   | ns   |
| $T_{r/f}$ | Rise time / fall time matching | $T_{r/f} = t_r / t_f$ | 90   | —    | 110  | %    |

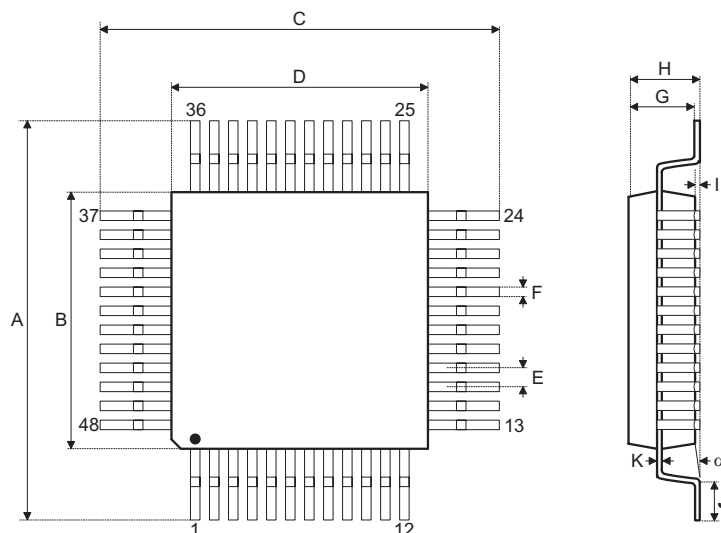
## 6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the [Holtek website](#) for the latest version of the [Package/Carton Information](#).

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

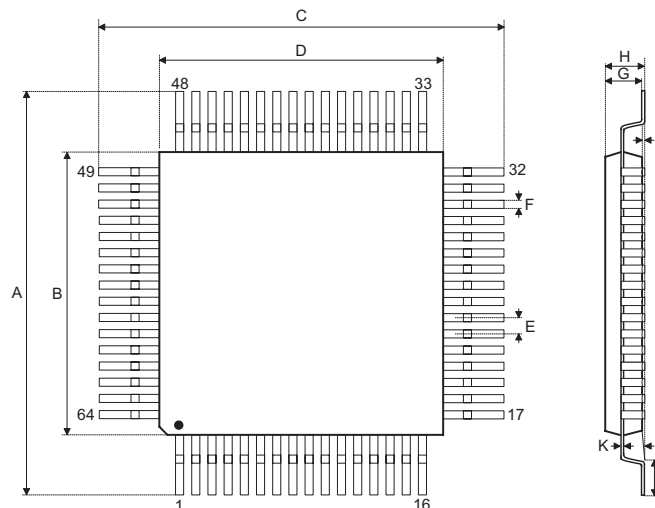
## 48-pin LQFP (7mm×7mm) Outline Dimensions



| Symbol | Dimensions in inch |           |       |
|--------|--------------------|-----------|-------|
|        | Min.               | Nom.      | Max.  |
| A      |                    | 0.354 BSC |       |
| B      |                    | 0.276 BSC |       |
| C      |                    | 0.354 BSC |       |
| D      |                    | 0.276 BSC |       |
| E      |                    | 0.020 BSC |       |
| F      | 0.007              | 0.009     | 0.011 |
| G      | 0.053              | 0.055     | 0.057 |
| H      | —                  | —         | 0.063 |
| I      | 0.002              | —         | 0.006 |
| J      | 0.018              | 0.024     | 0.030 |
| K      | 0.004              | —         | 0.008 |
| α      | 0°                 | —         | 7°    |

| Symbol | Dimensions in mm |          |      |
|--------|------------------|----------|------|
|        | Min.             | Nom.     | Max. |
| A      |                  | 9.00 BSC |      |
| B      |                  | 7.00 BSC |      |
| C      |                  | 9.00 BSC |      |
| D      |                  | 7.00 BSC |      |
| E      |                  | 0.50 BSC |      |
| F      | 0.17             | 0.22     | 0.27 |
| G      | 1.35             | 1.40     | 1.45 |
| H      | —                | —        | 1.60 |
| I      | 0.05             | —        | 0.15 |
| J      | 0.45             | 0.60     | 0.75 |
| K      | 0.09             | —        | 0.20 |
| α      | 0°               | —        | 7°   |

## 64-pin LQFP (7mm×7mm) Outline Dimensions



| Symbol | Dimensions in inch |           |       |
|--------|--------------------|-----------|-------|
|        | Min.               | Nom.      | Max.  |
| A      |                    | 0.354 BSC |       |
| B      |                    | 0.276 BSC |       |
| C      |                    | 0.354 BSC |       |
| D      |                    | 0.276 BSC |       |
| E      |                    | 0.016 BSC |       |
| F      | 0.005              | 0.007     | 0.009 |
| G      | 0.053              | 0.055     | 0.057 |
| H      | —                  | —         | 0.063 |
| I      | 0.002              | —         | 0.006 |
| J      | 0.018              | 0.024     | 0.030 |
| K      | 0.004              | —         | 0.008 |
| α      | 0°                 | —         | 7°    |

| Symbol | Dimensions in mm |          |      |
|--------|------------------|----------|------|
|        | Min.             | Nom.     | Max. |
| A      |                  | 9.00 BSC |      |
| B      |                  | 7.00 BSC |      |
| C      |                  | 9.00 BSC |      |
| D      |                  | 7.00 BSC |      |
| E      |                  | 0.40 BSC |      |
| F      | 0.13             | 0.18     | 0.23 |
| G      | 1.35             | 1.40     | 1.45 |
| H      | —                | —        | 1.60 |
| I      | 0.05             | —        | 0.15 |
| J      | 0.45             | 0.60     | 0.75 |
| K      | 0.09             | —        | 0.20 |
| α      | 0°               | —        | 7°   |

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